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Abel / Totoro MS-7040 *Rev. 110*

Intel (R) Springdale (GMCH) + ICH5 Chipset
Intel Northwood & Prescott mPGA478B Processor

CPU:

Intel Northwood/Prescott - 3.0G & Above

System Chipset:

Intel Springdale - GMCH (North Bridge)
Intel ICH5 (South Bridge)

On Board Chipset:

BIOS -- FWH EEPROM 4M
AC'97 Codec -- STAC9752T
LPC Super I/O -- W83627THF
LAN - Intel 82562EZ (10/100)
1394 -- NEC PD72874
CLOCK -- Cypress CY28405

Main Memory:

DDR * 4 (Max 4GB)

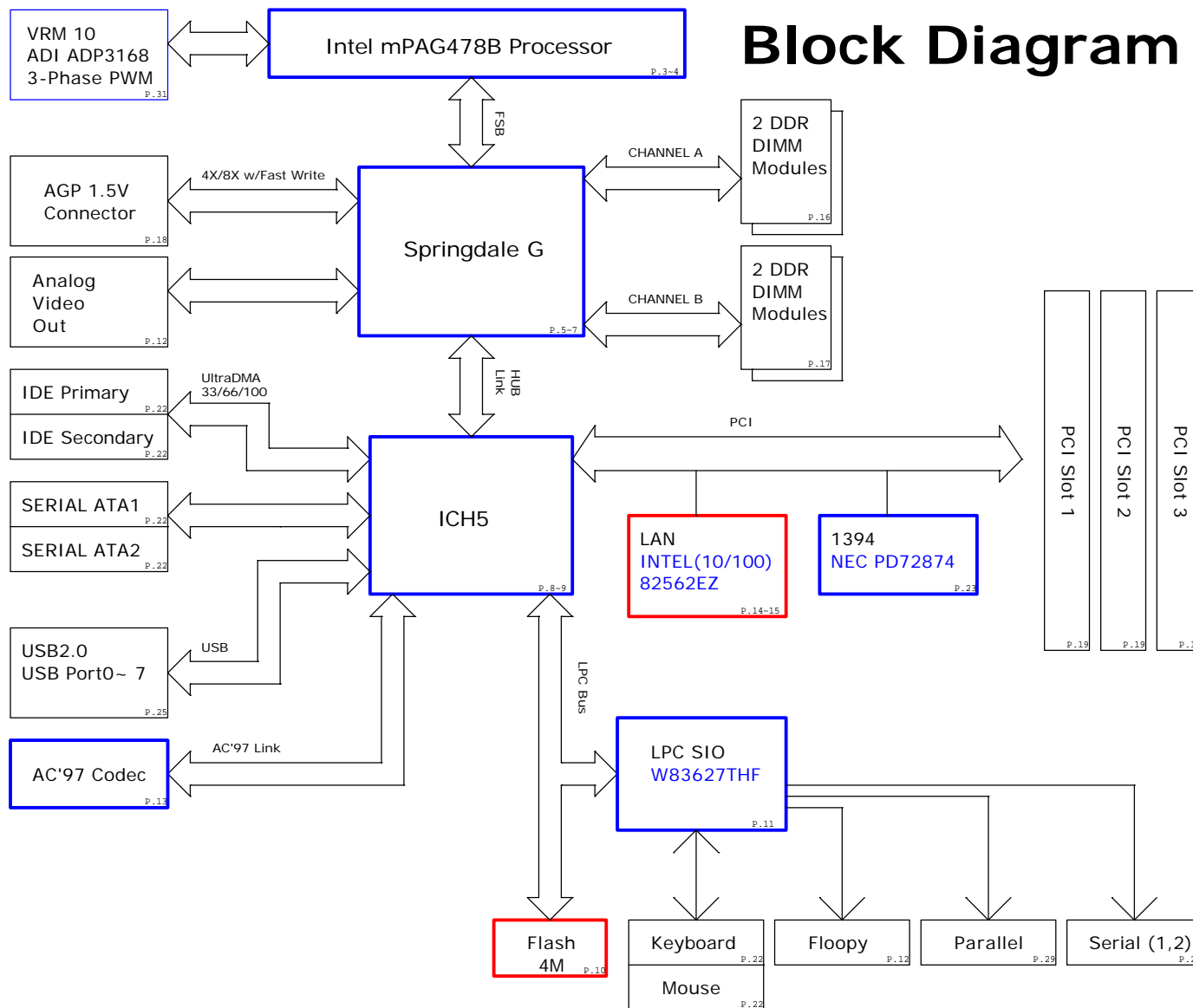
Expansion Slots:

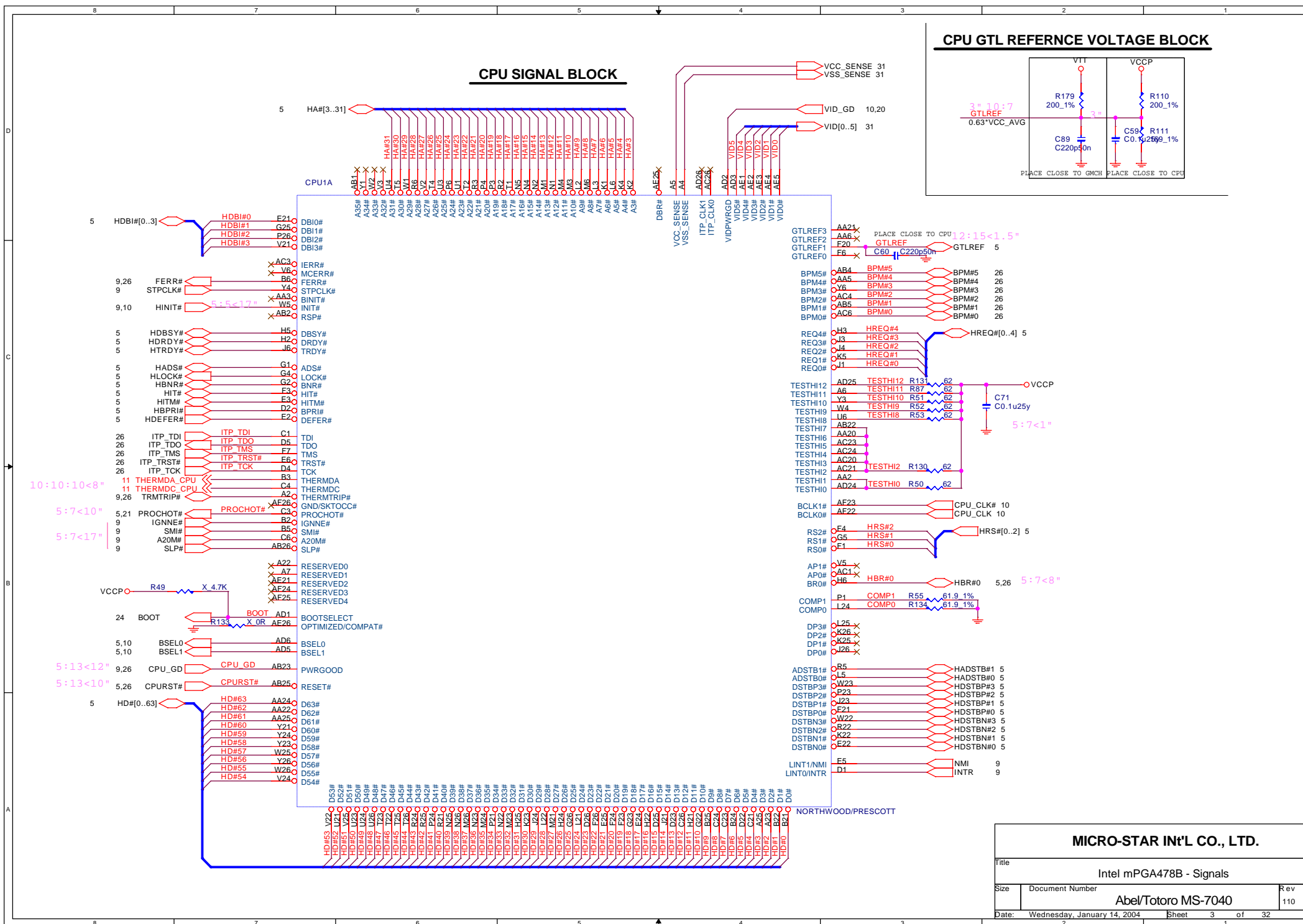
PCI2.3 SLOT * 3
AGP4X/8X SLOT * 1

ADI PWM:

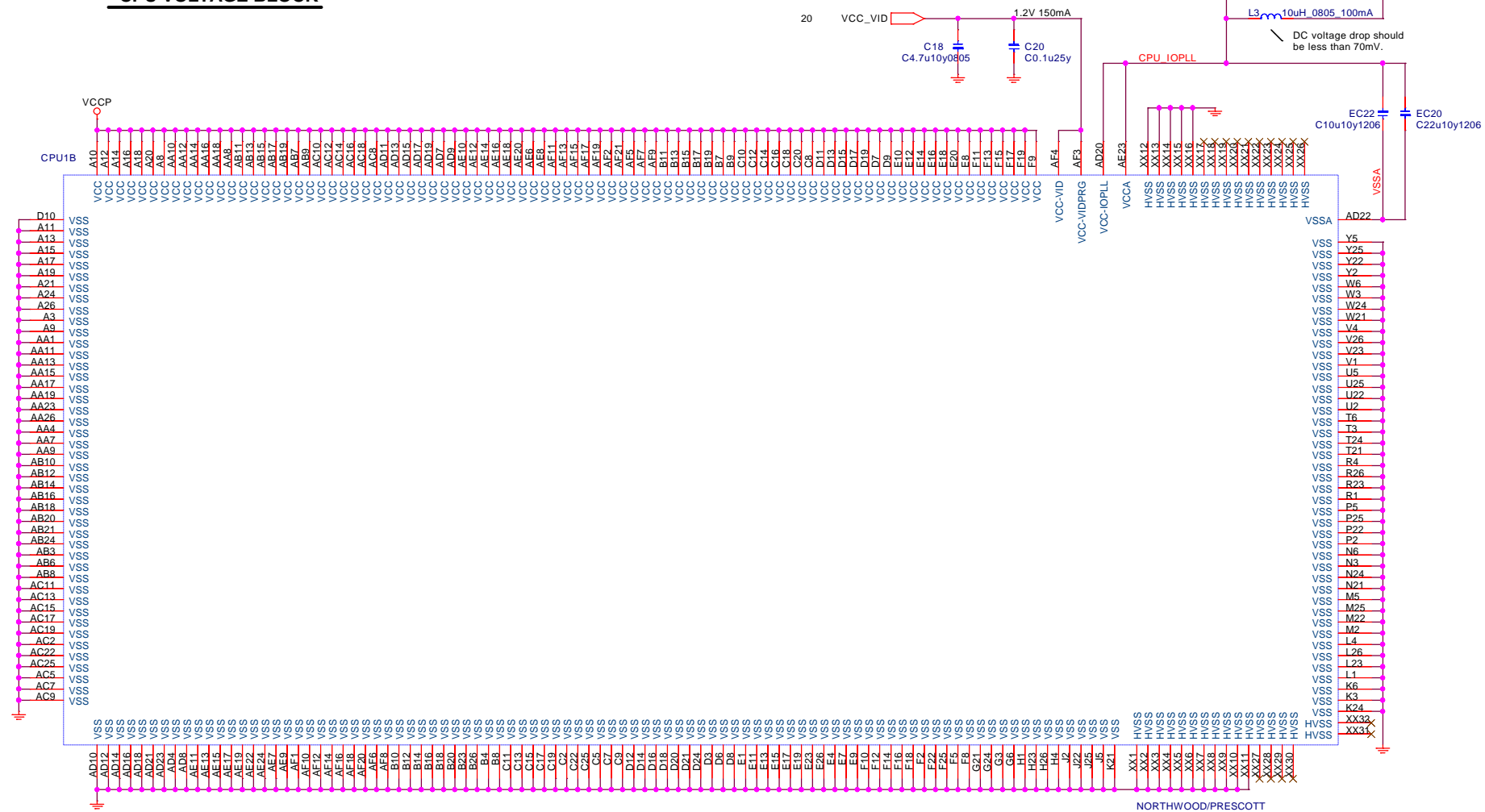
Controller: ADP3168
Driver: ADP3418 * 3

MICRO-STAR INT'L CO., LTD.			
Title			
COVER SHEET			
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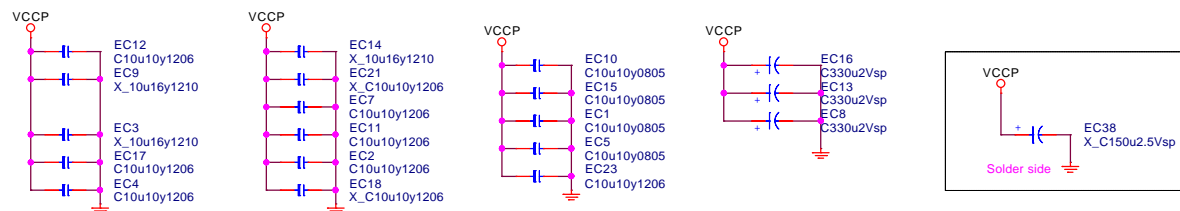




CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



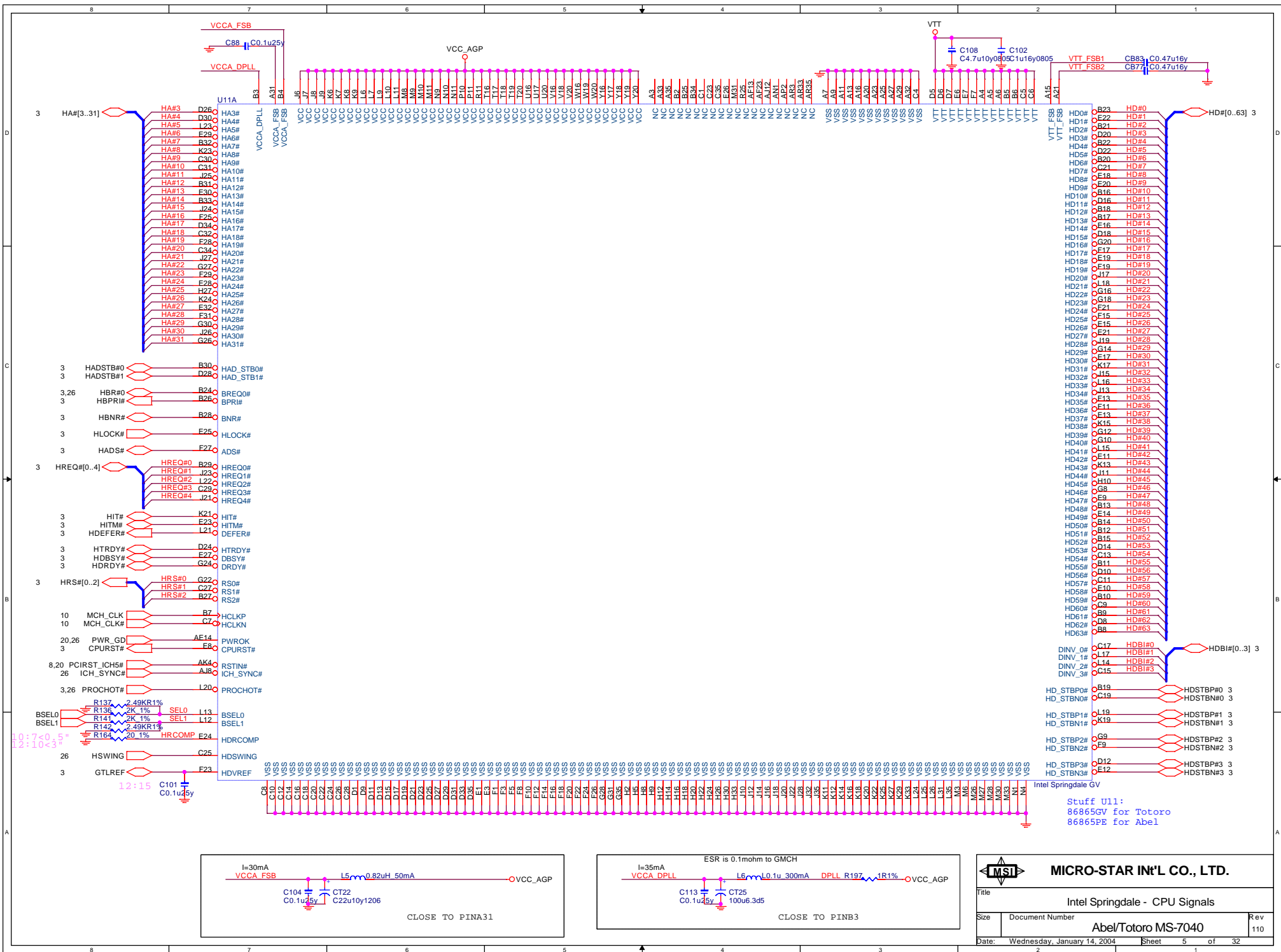
MICRO-STAR INT'L CO., LTD.

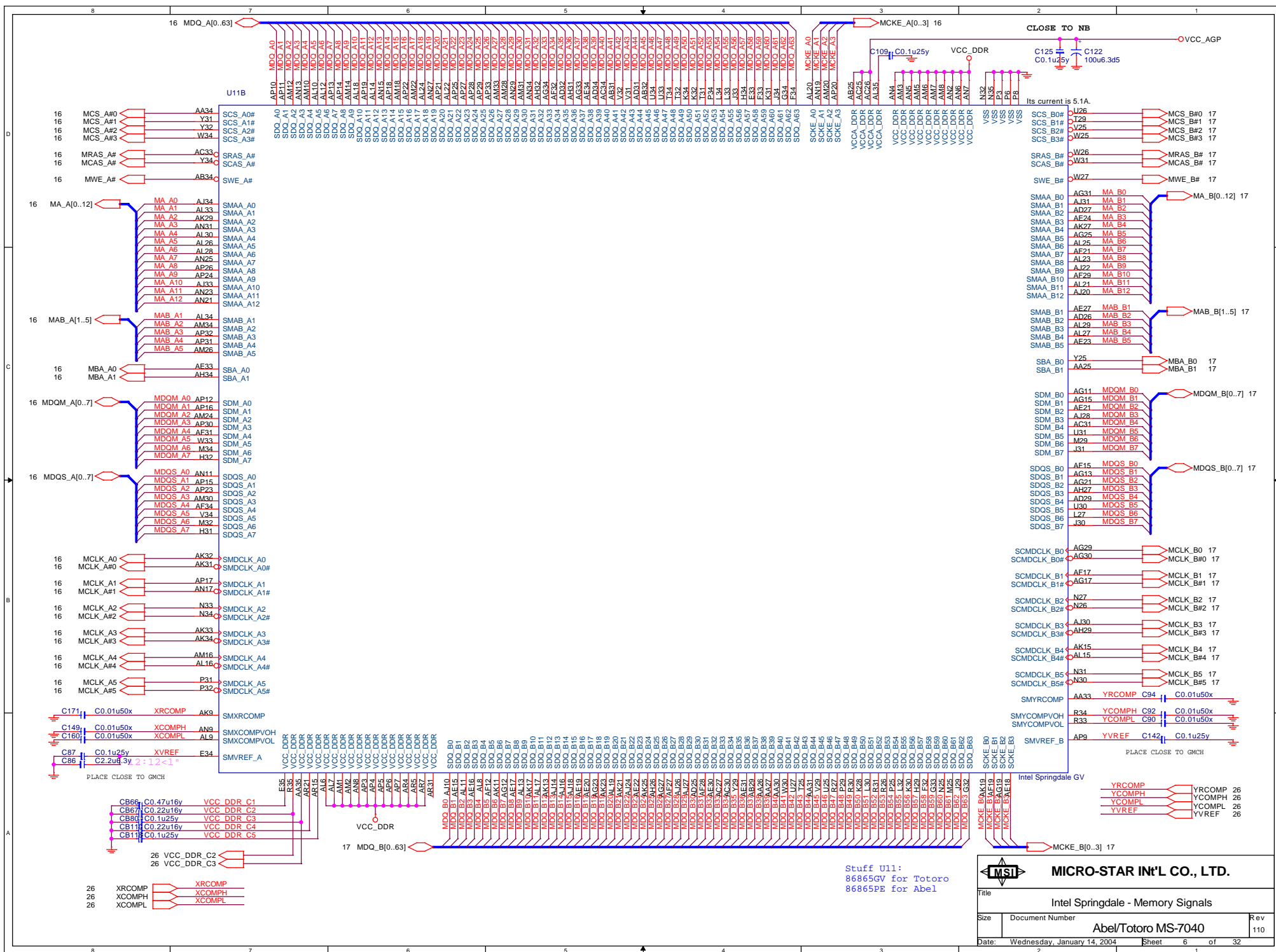
Intel mPGA478B - Power

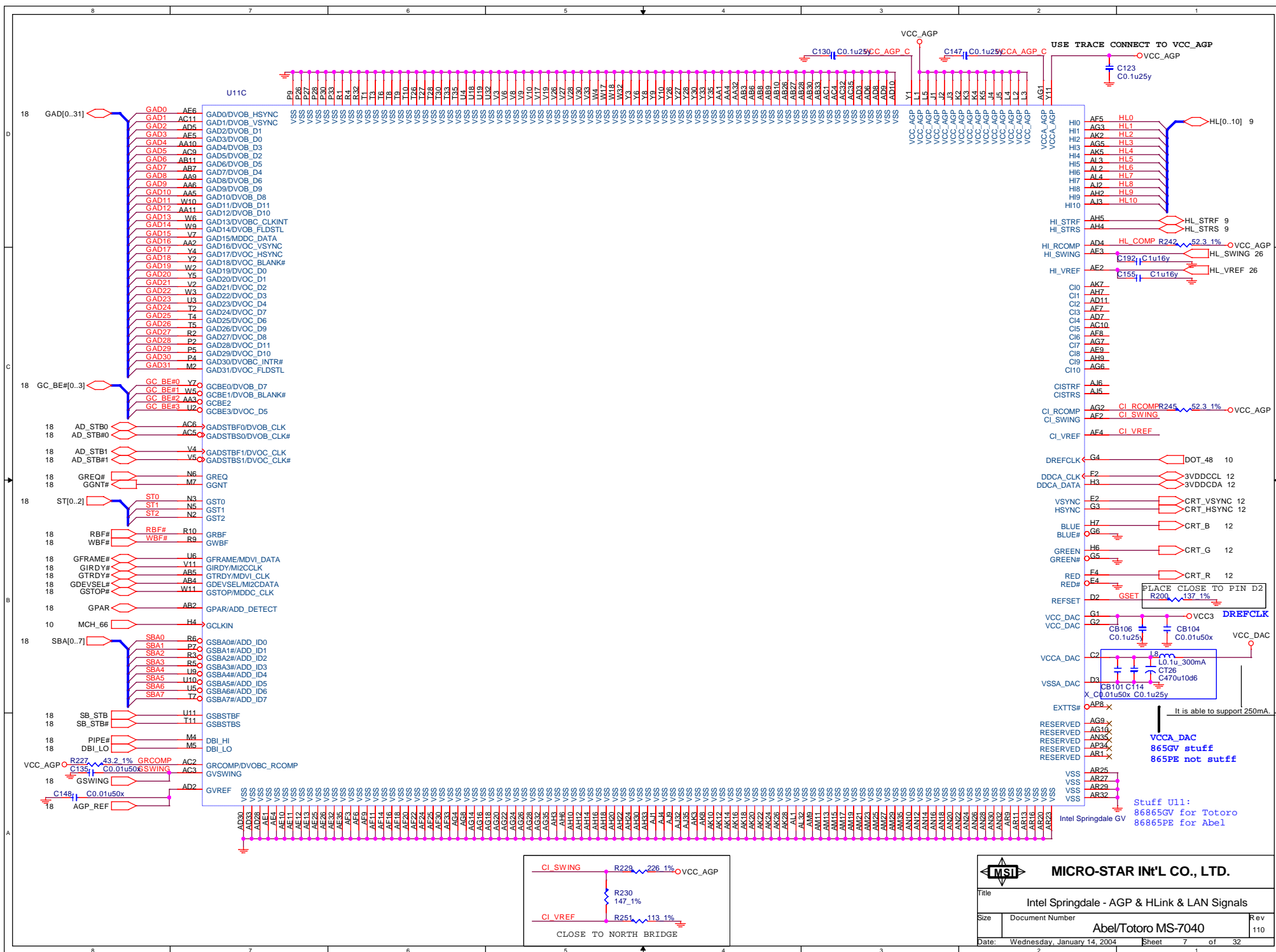
Abel/Totoro MS-7040

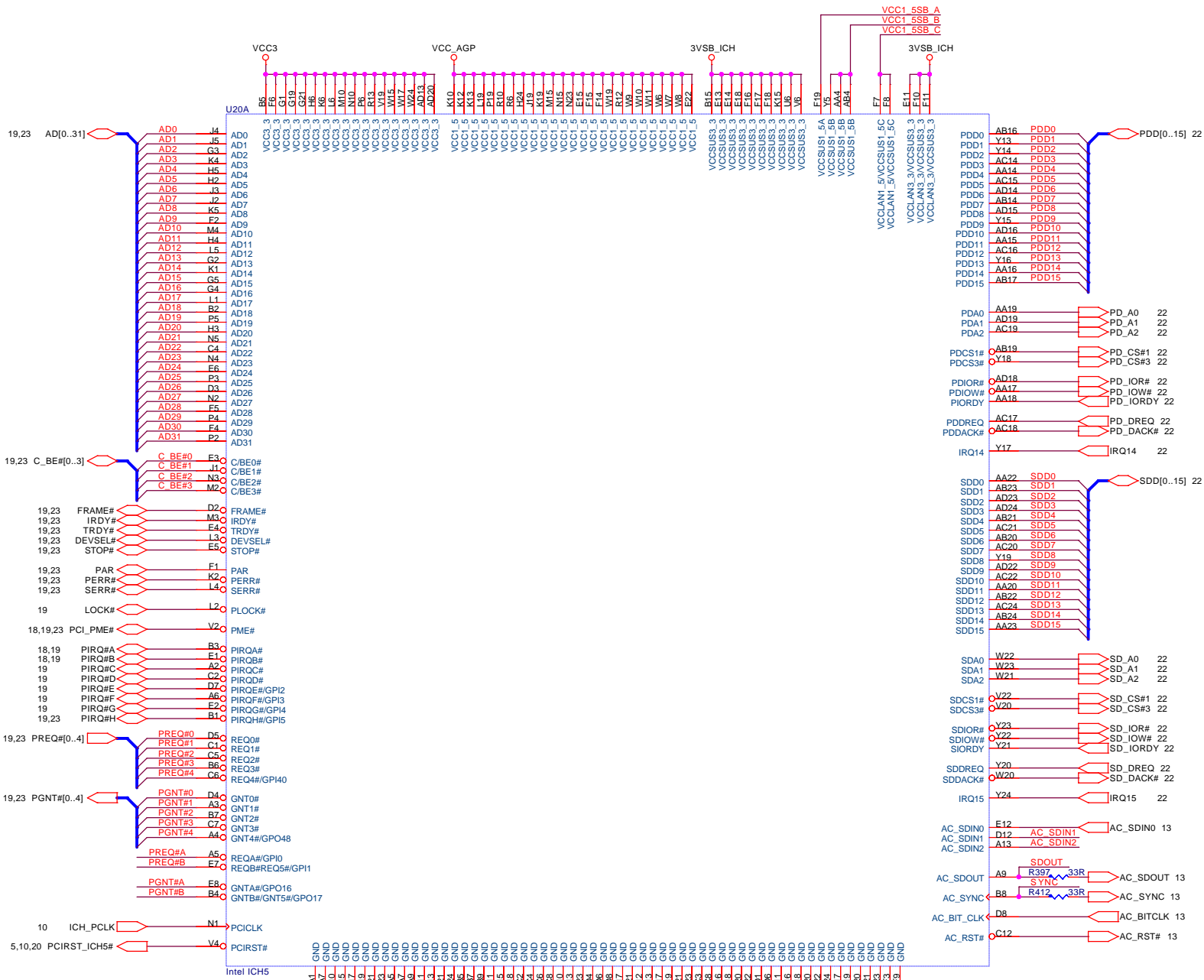
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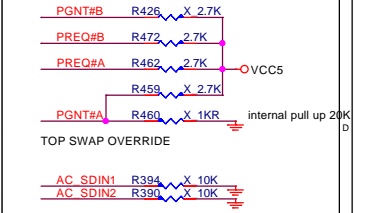




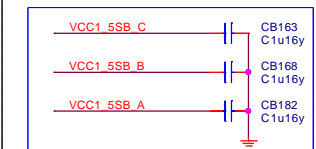
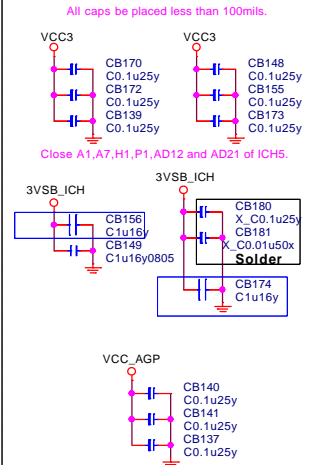




ICH5 Pull-Up / Down Resistors

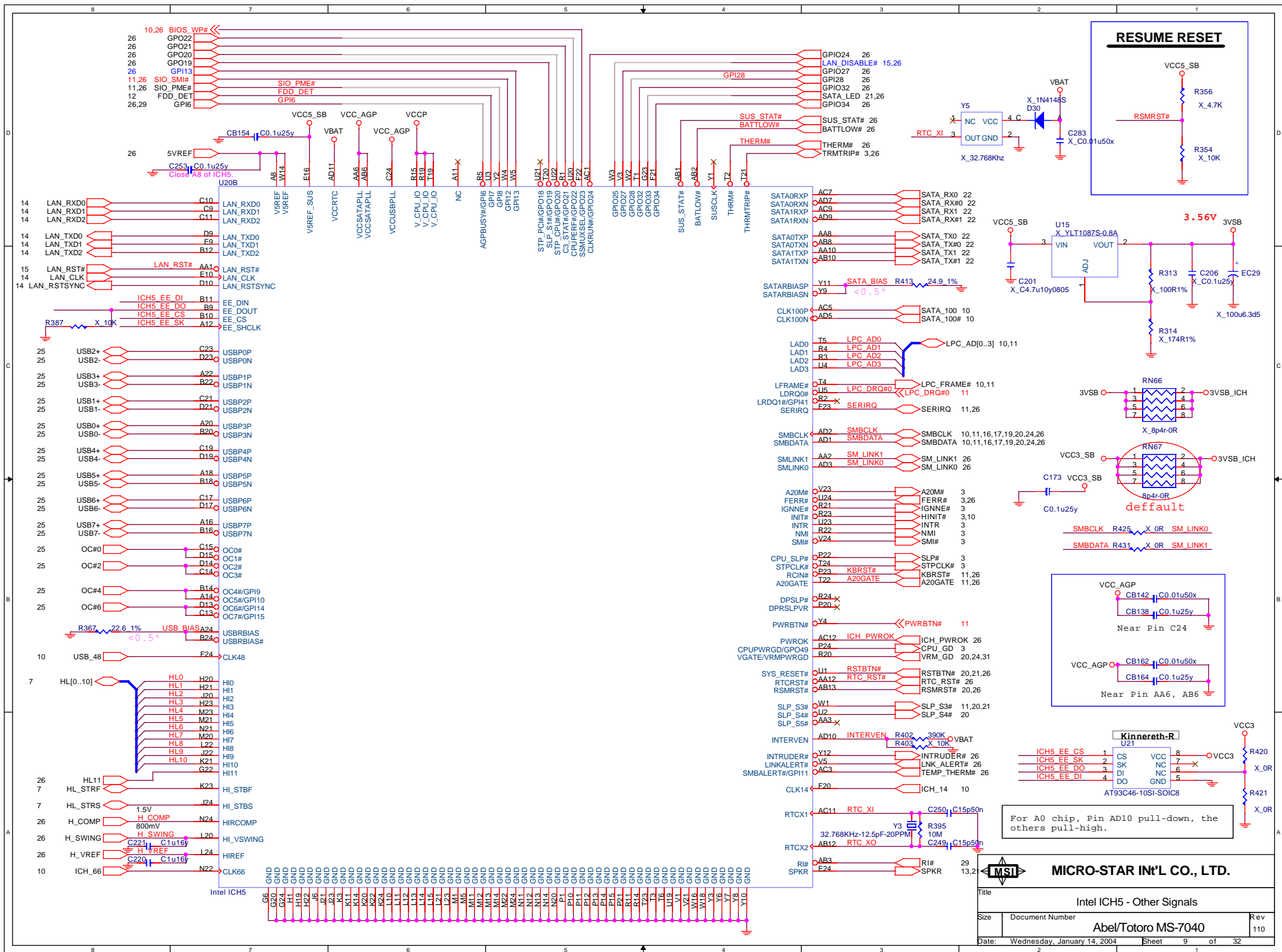


ICH5 Decoupling Capacitors

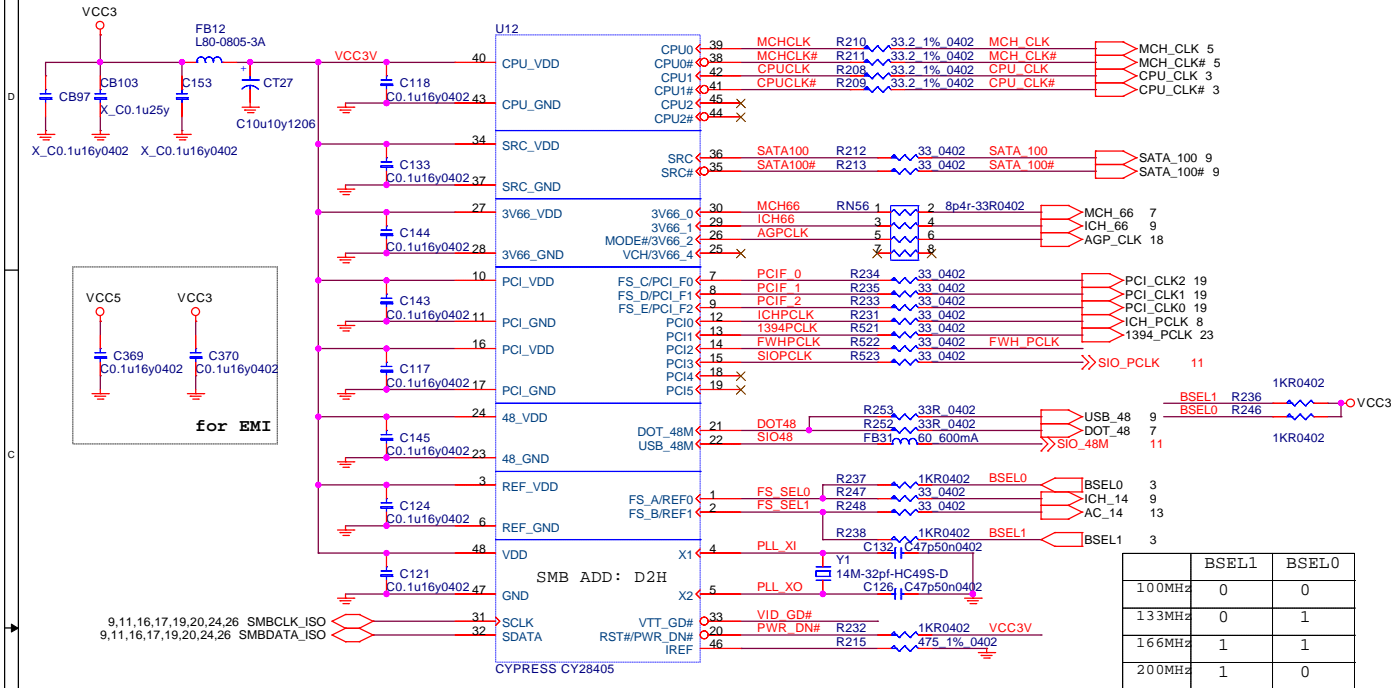


MICRO-STAR INT'L CO., LTD.

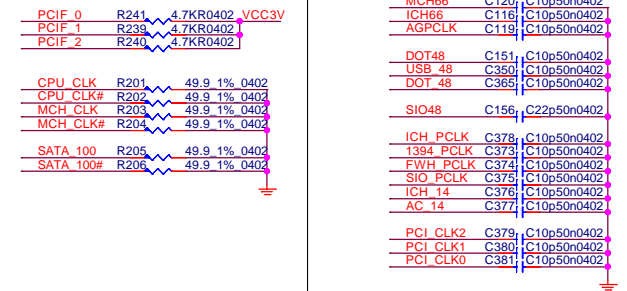
Title		Intel ICH5 - PCI & IDE & AC97 Signals	
Size	Document Number	Abel/Totoro MS-7040	Rev 110
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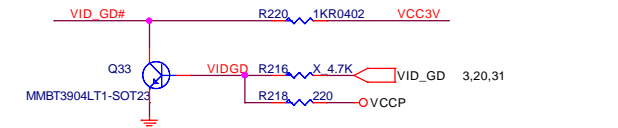
CLOCK GENERATOR



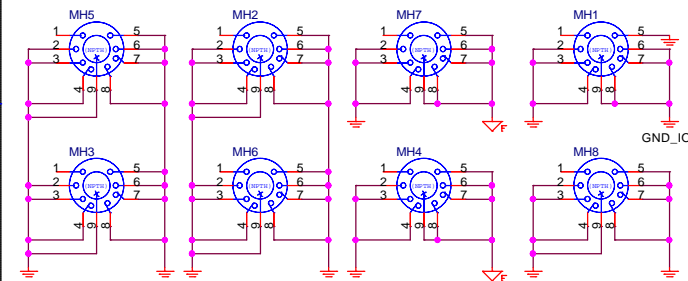
EMC HF filter capacitors, located close to PLL



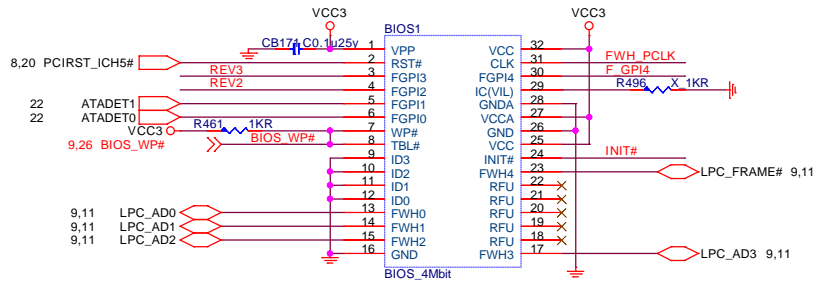
CLOCK GENERATOR VTT POWER DOWN BLOCK



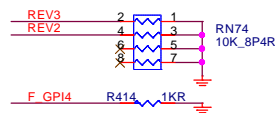
Mounting Holes



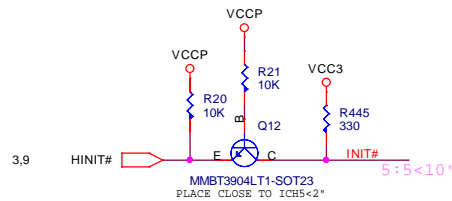
FIRMWARE HUB (FWH)



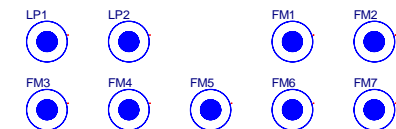
FWH RESISTORS



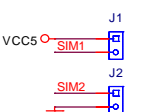
FWH INIT Signal Voltage Translation



Optics Orientation Holes



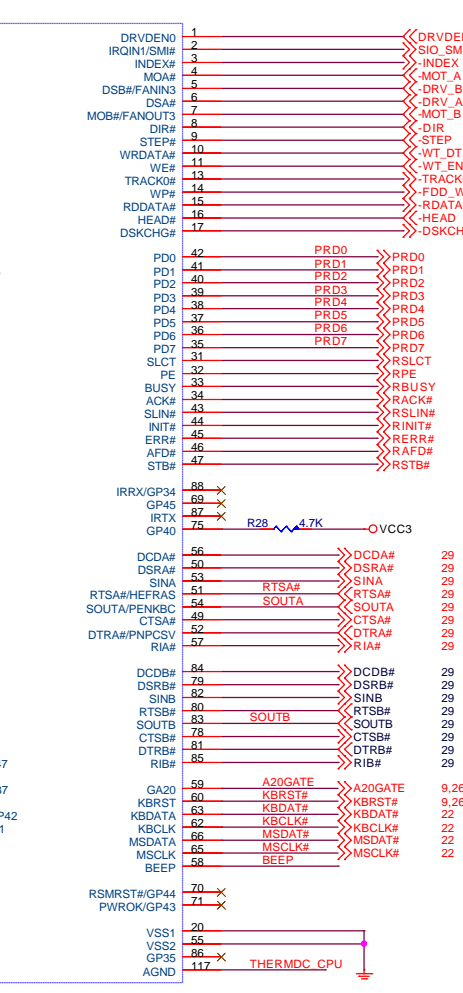
Simulation



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Title			CY28405 & FWH
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		U6	
20	PCIRST#1	30	LRESET#
10	SIO_PCLK	21	CLCK
9,26	SERRIO	23	SERRQ
9	LPC_DRQ0#	28	LDQ0#
9,10	LPC_FRAME#	29	LFRAME#
9,10	LPC_AD0	27	LAD0
9,10	LPC_AD1	26	LAD1
9,10	LPC_AD2	25	LAD2
9,10	LPC_AD3	24	LAD3



VCC5 ○ R5 4.7K SOUTA

VCC5 ○ R64 4.7K SOUTB

R60 X 4.7K

RTSA#

VCC5 ○ R6 X 4.7K

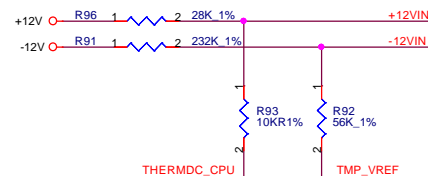
SPEAKER BLOCK

SPEAKER BLOCK

The diagram shows a circuit for a speaker block. It includes a VCC5 supply, a 10K resistor (R9), a 4.7K resistor (R10), and a transistor (Q19, MMBT3904LT1-SOT23). The BEEP input is connected to R9 and R10. The ALARM output is connected to the collector of Q19.

NOTE: LOCATE CLOSE STATUS PANEL

**NOTE: LOCATE CLOSE
STATUS PANEL**



Title

LPC SUPER I/O

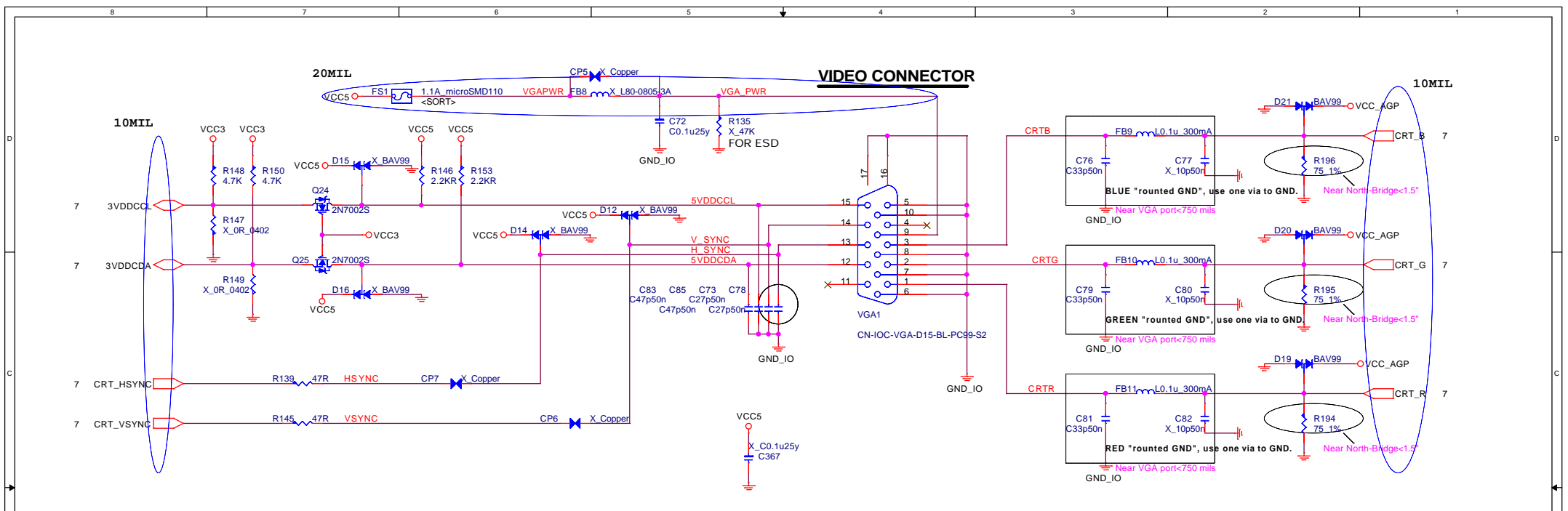
Size

Document Number

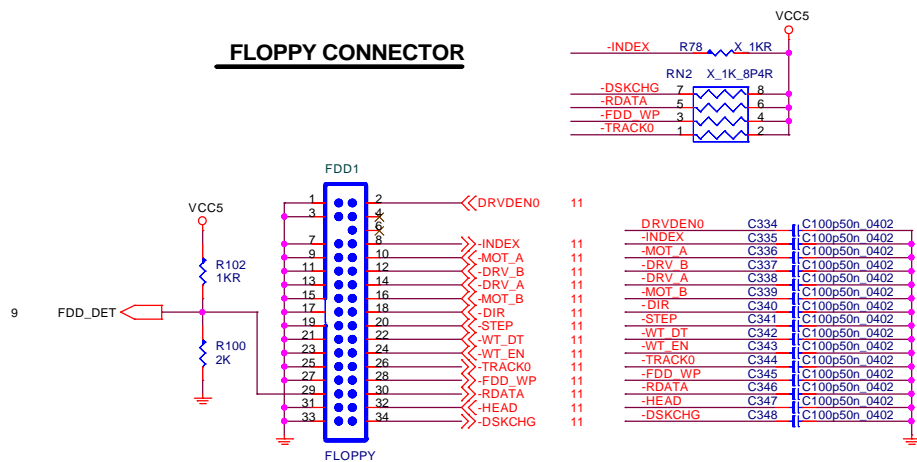
Abel/Totoro MS-7040

110

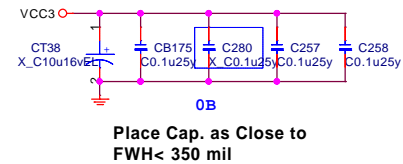
Date: Wednesday, January 14, 2004 Sheet 11 of 32



FLOPPY CONNECTOR



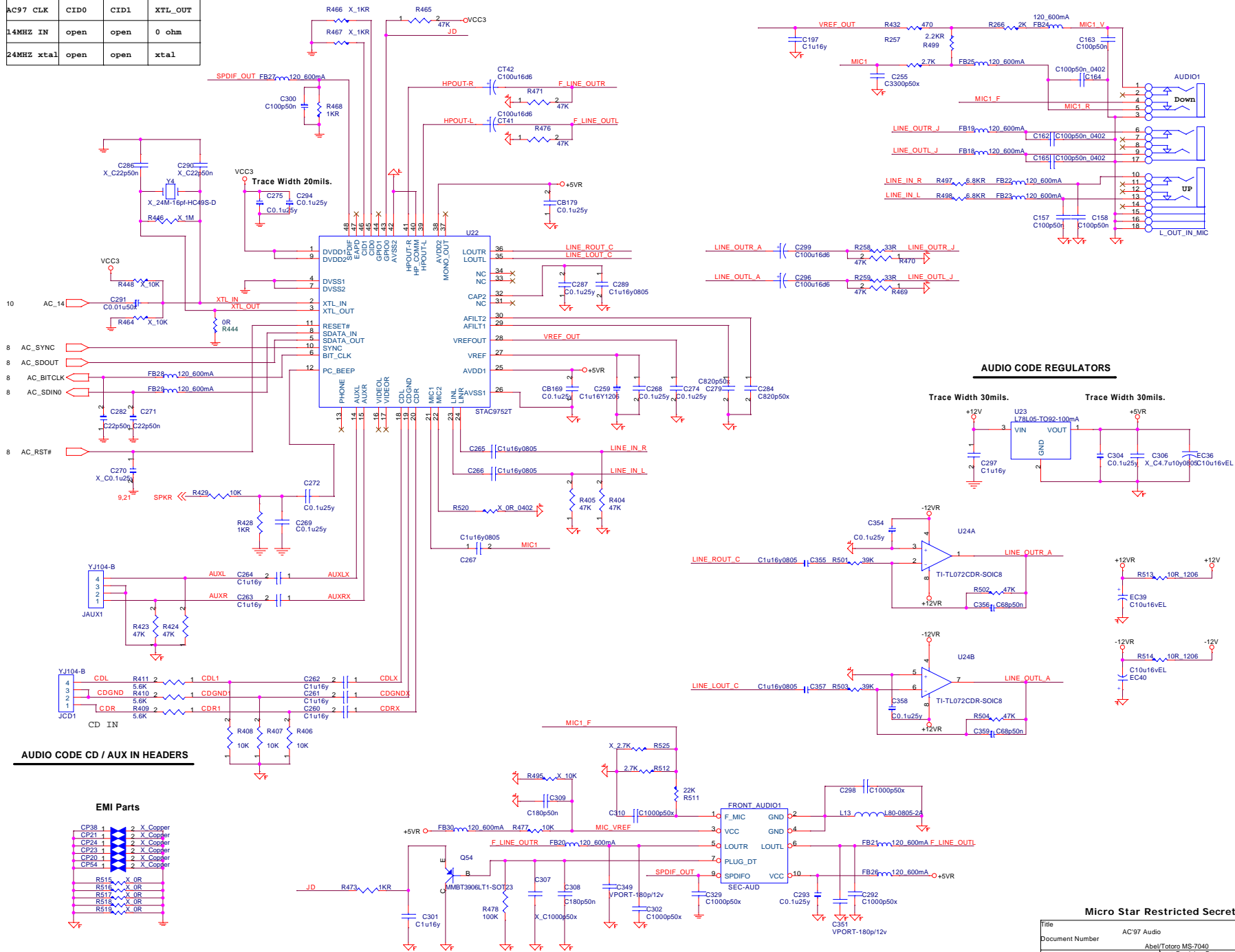
FWH DECOUPLING CAPACITORS



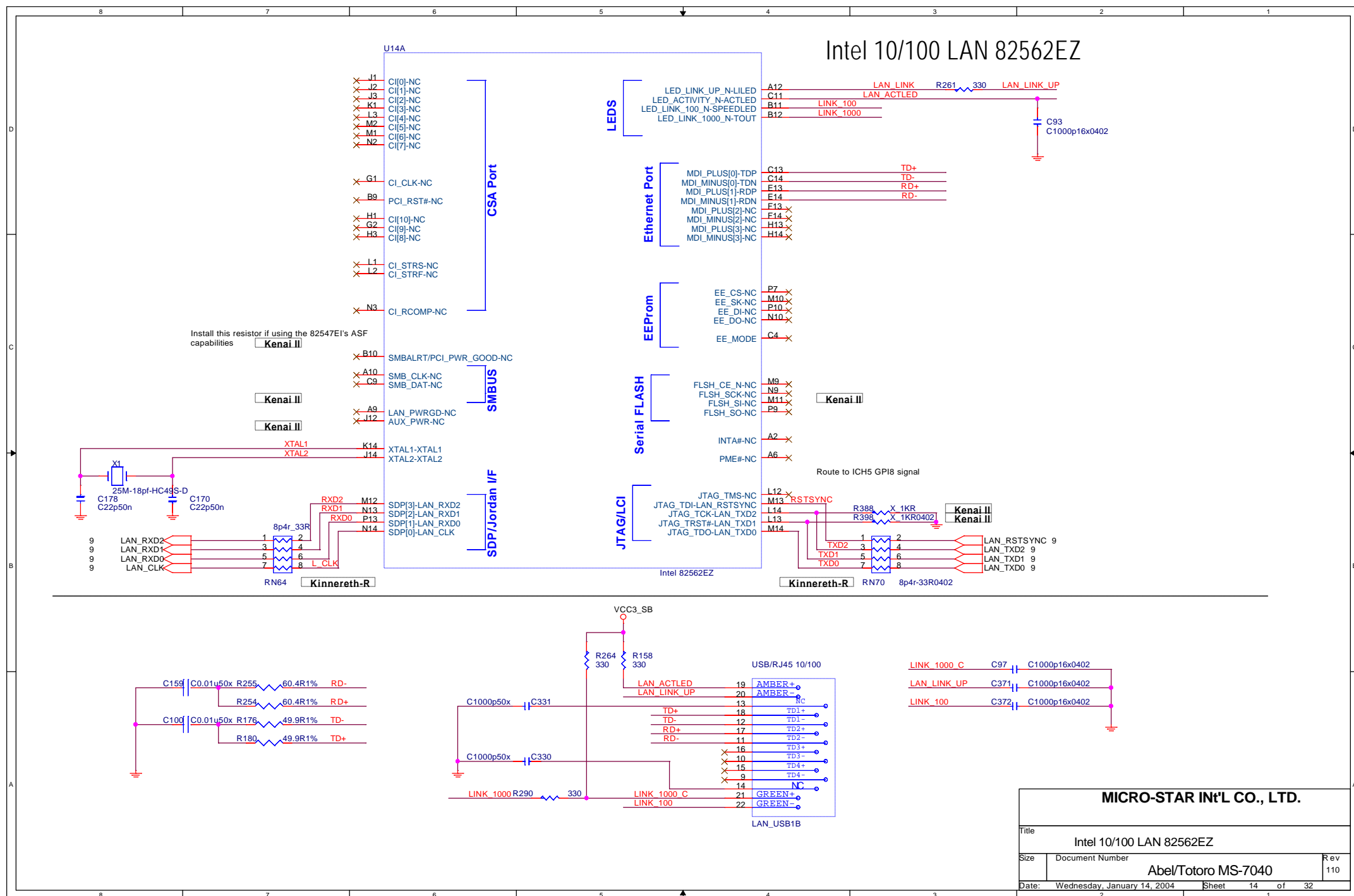
MICRO-STAR INT'L CO., LTD.

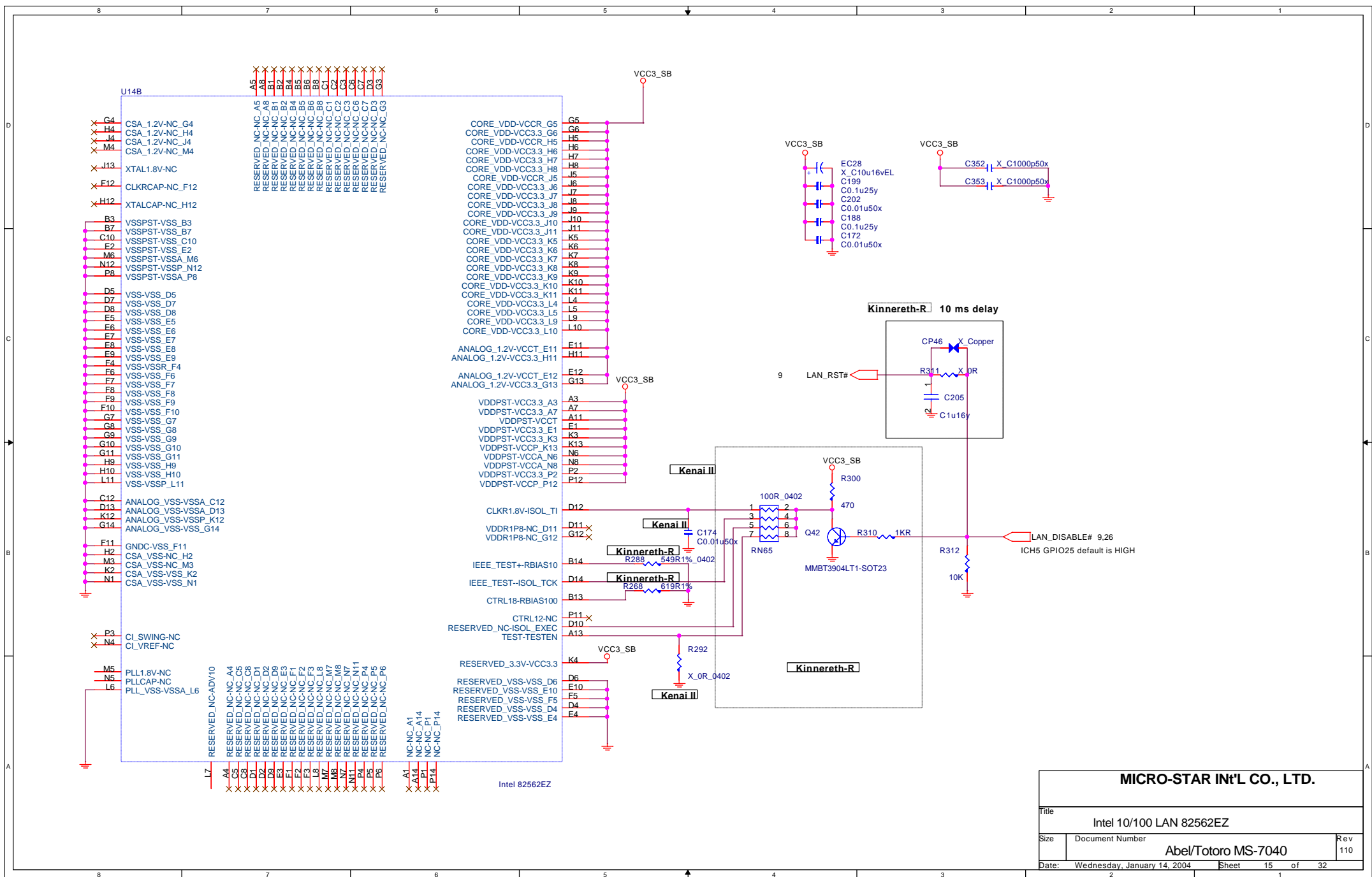
Title			FLOPPY & VGA CONNECTOR	
Size	Document Number			Rev
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AC97 CLK	CID0	CID1	XTL_OUT
14MHZ IN	open	open	0 ohm
24MHZ xtal	open	open	xtal



Title	AC'97 Audio	Rev	110
Document Number	AbelTotoro MS-7040		
MICRO-STAR INT'L CO.,LTD.	Last Revision Date:		
No. 69, Li-De St. Jung-He City,	Wednesday, January 14, 2004		
Taipei Hsein, Taiwan			
http://www.msi.com.tw	Sheet	13	of 32





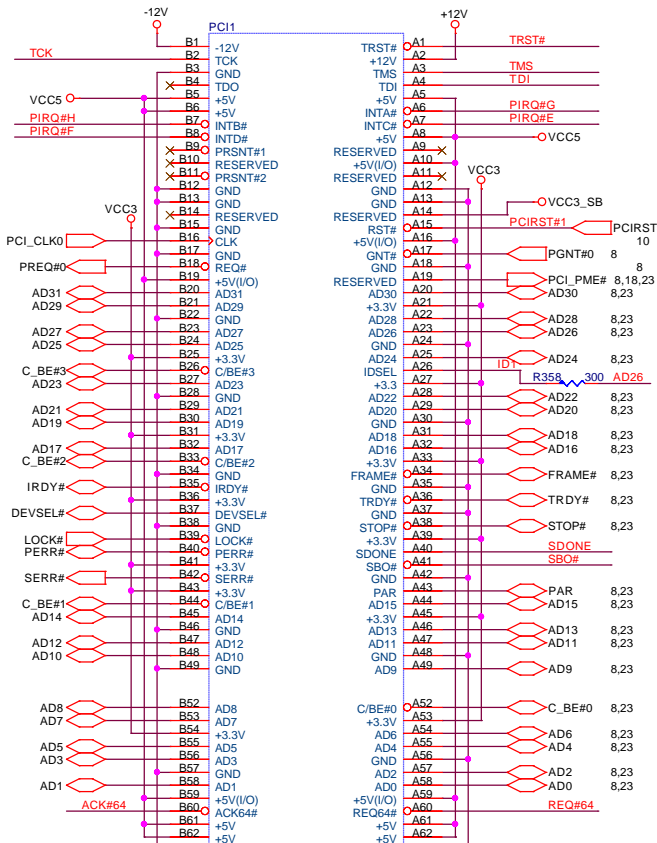
VCC5 = 60mils trace / 15 mils space

VCCg	8.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	0.75A

AGP1

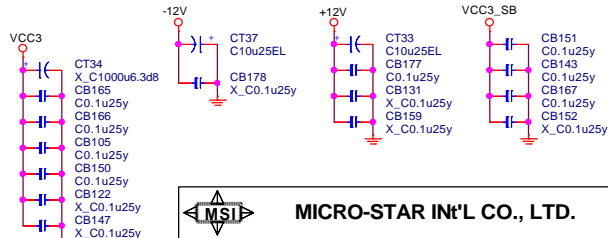
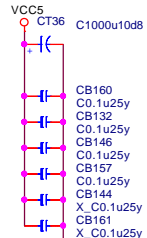
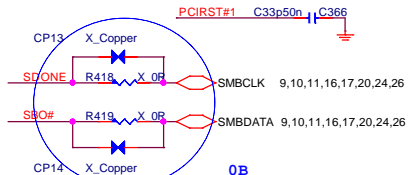
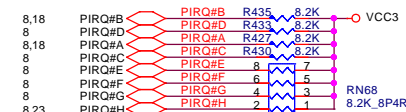
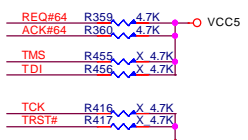
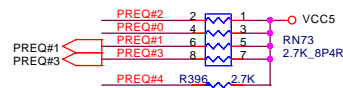
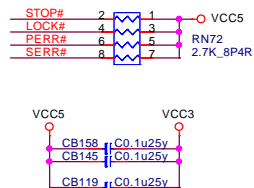


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[illegible]

FRAME# 2 1
IRDY# 4 3
TRDY# 6 5
DEVSEL# 8 7

VCC5
RN71
2.7K_8P4R
8
8



Abel/Totoro MS-7040

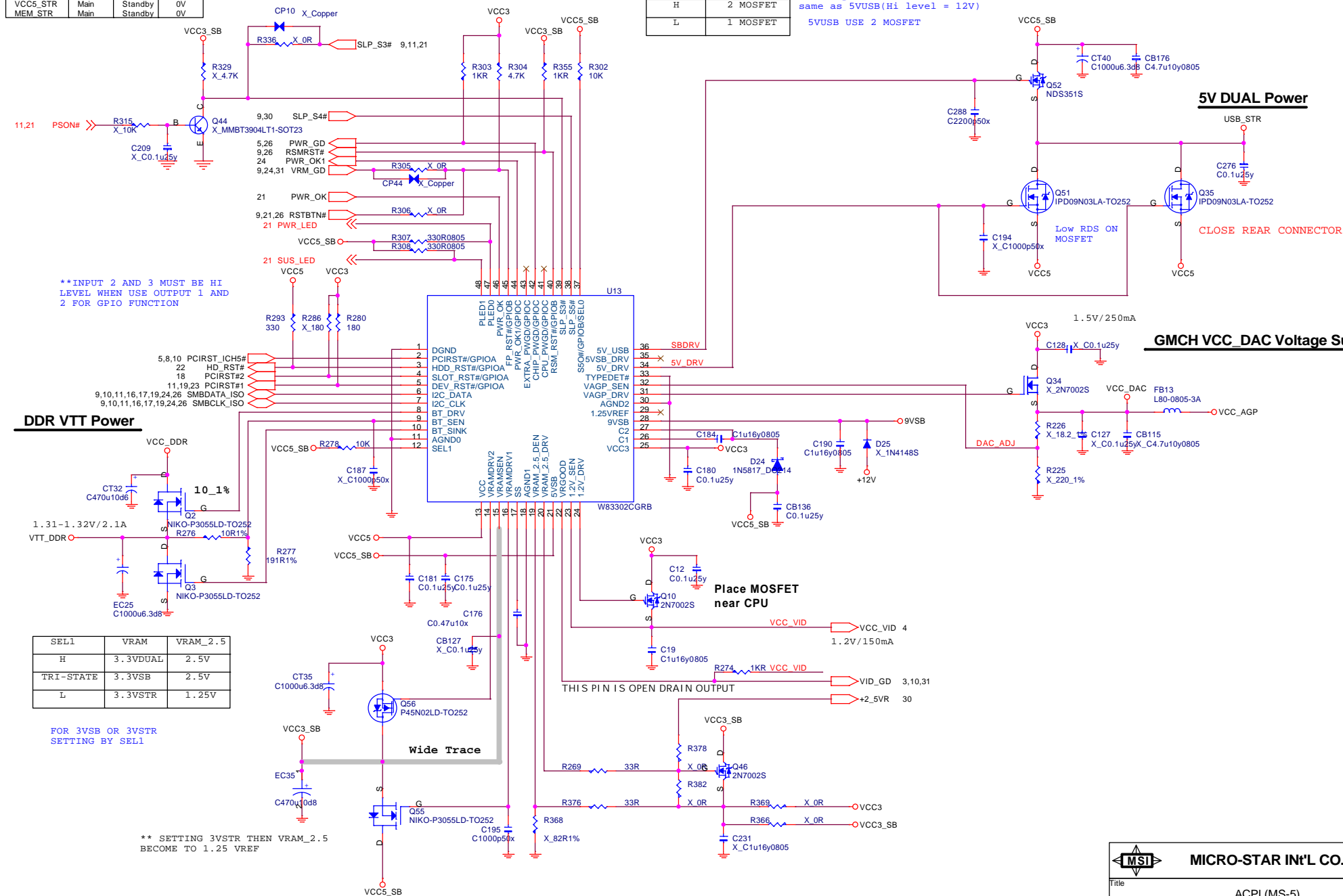
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Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

```
**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)


5VUSB USE 2 MOSFET
```



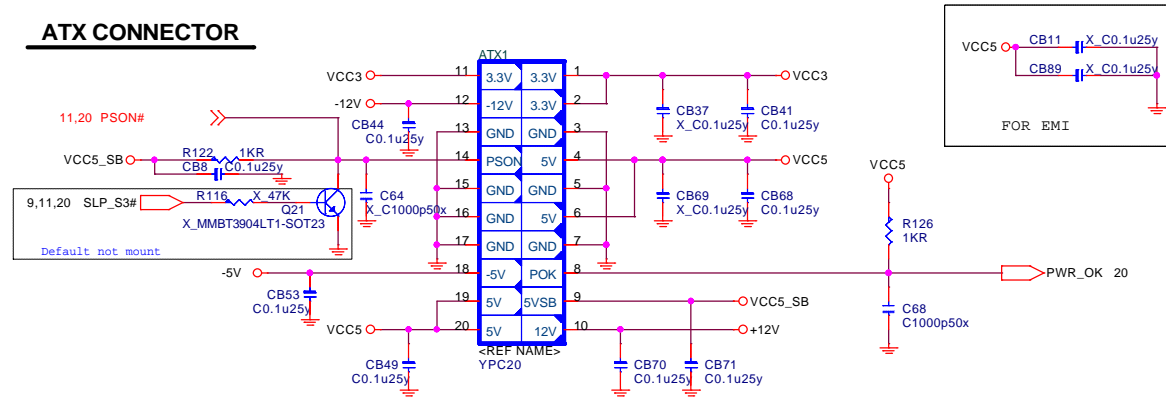
SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

```
** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF
```

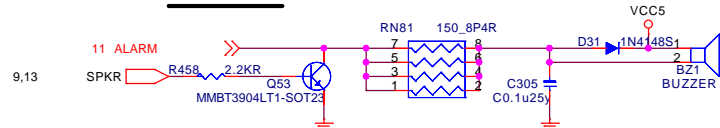
 MICRO-STAR INT'L CO., LTD.	
Title	
ACPI (MS-5)	
Size	Document Number
	Abel/Totoro MS-7040
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ATX CONNECTOR

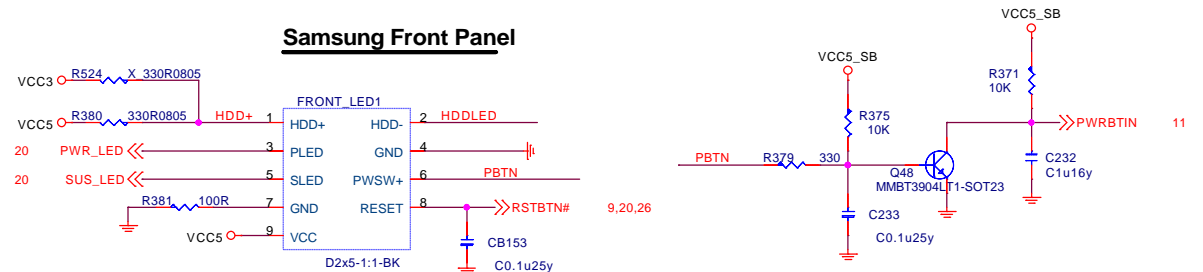


*Placement close to ATX connect.

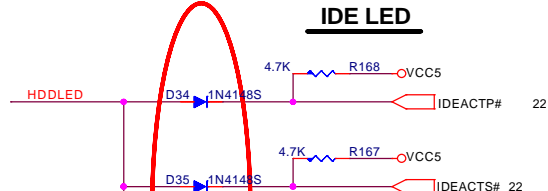
BUZZER



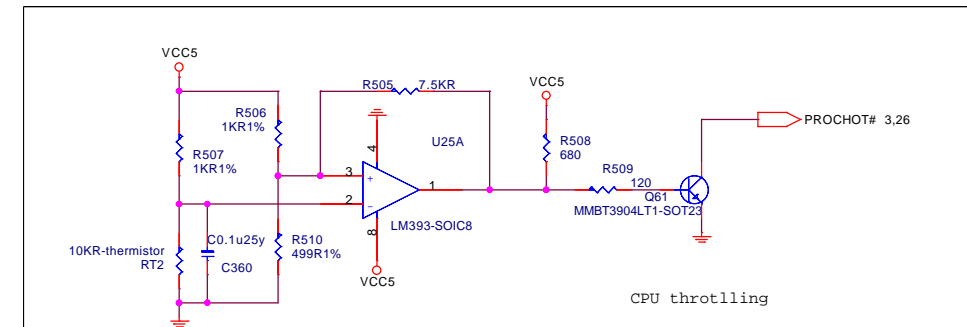
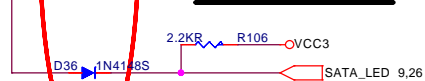
Samsung Front Panel



IDE LED



SERIAL ATA LED

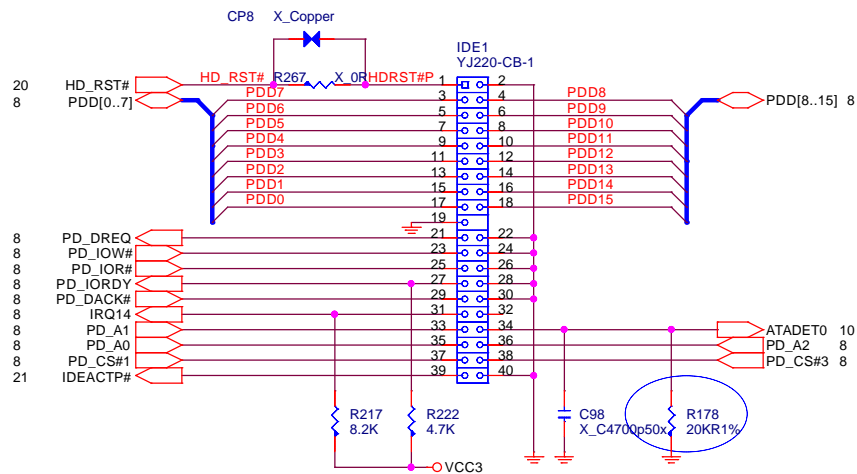


MICRO-STAR INT'L CO., LTD.

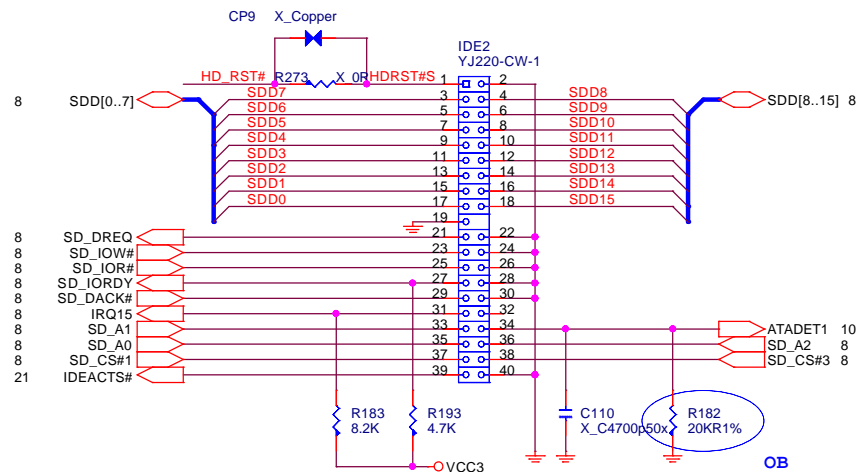
Title			ATX Connector & Front Panel & Buzzer	
Size	Document Number		Abel/Totoro MS-7040	
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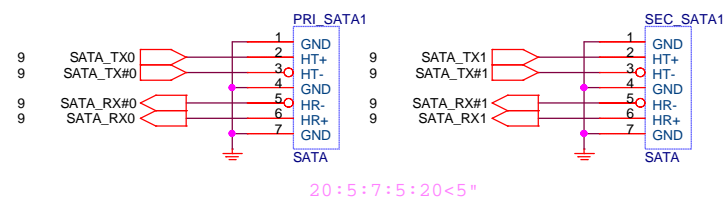
PRIMARY IDE BLOCK



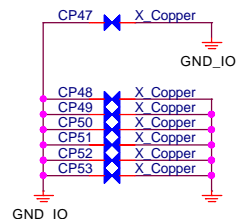
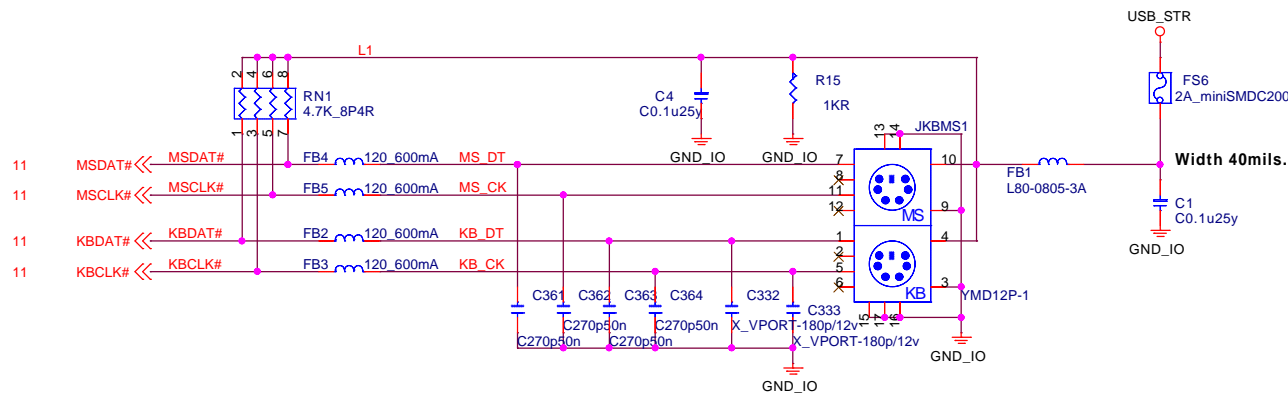
SECONDARY IDE BLOCK



SERIAL ATA CONNECTOR BLOCK



PS2 KEYBOARD & MOUSE CONNECTOR

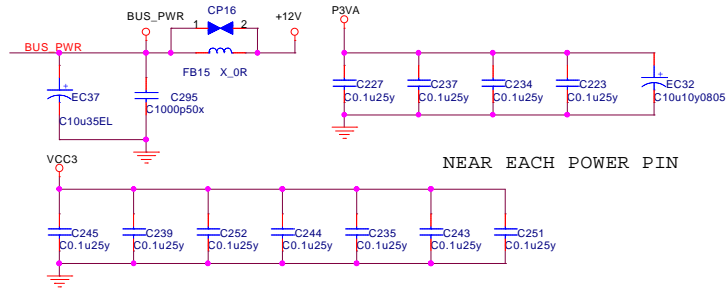


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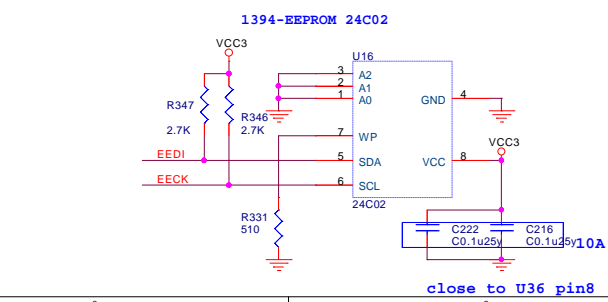
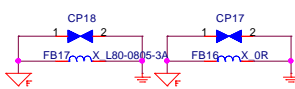
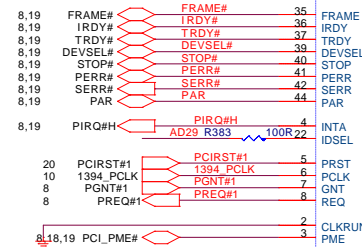
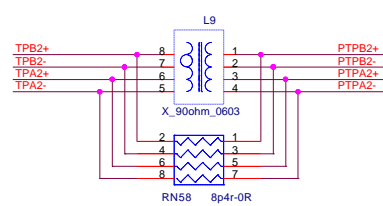
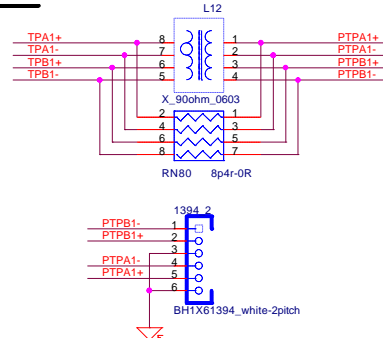
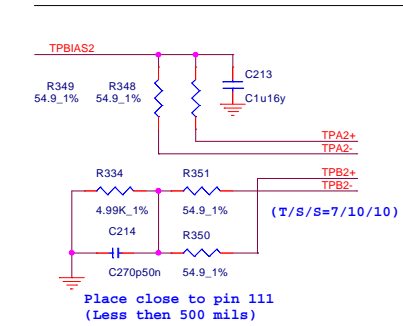
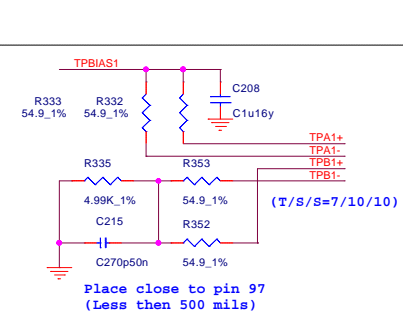
Title			PS2, IDE, SATA Connectors
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IEEE-1394

support S3 wake-up



FRONT 1394 PORT 1



AD29
INT#

AD[31:0]
C_BE#[3:0]

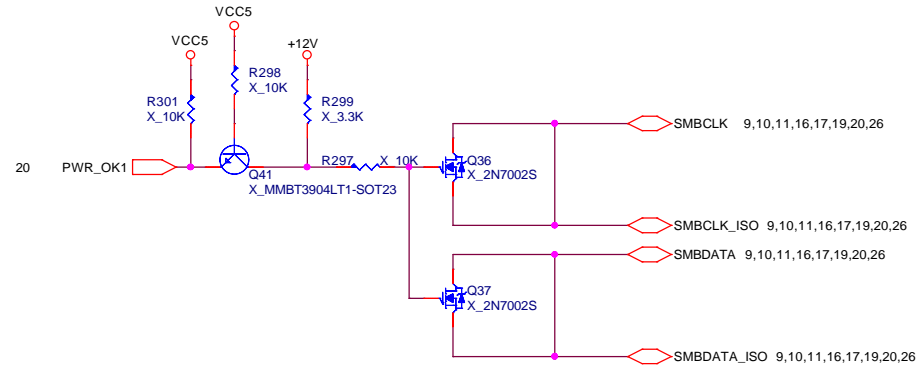
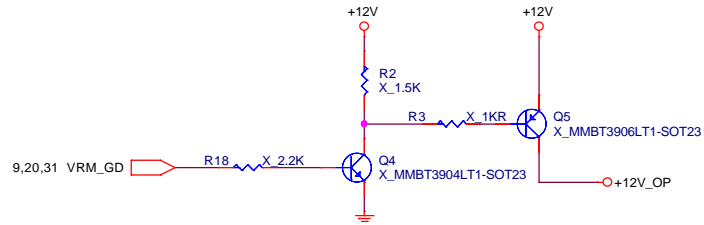
MICRO-STAR

NEC 1394

Abel/Totoro MS-7040

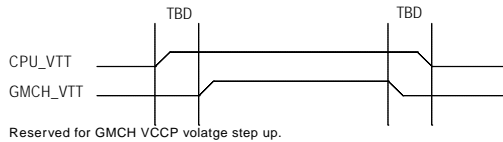
NOTE:
1. ASIC TO PHY MAX Length is less than 13.0 mm.
2. TPA0+ & TPA0- TWISTED LENGTH IS SAME. (Tolerance+4%)
3. TPB0+ & TPB0- TWISTED LENGTH IS SAME. (Tolerance+4%)
4. TRACE WIDTH= 7MIL
5. TPA0 & TPB0 impedance is 560±1%
6. TRACE SHALL AS SOME LAYER AND BETWEEN CROSS WITH GND
7. TPA0+, TPA0- & TPB0+, TPB0-, trace must be on surface

GMCH_VTT ON/OFF CIRCUIT

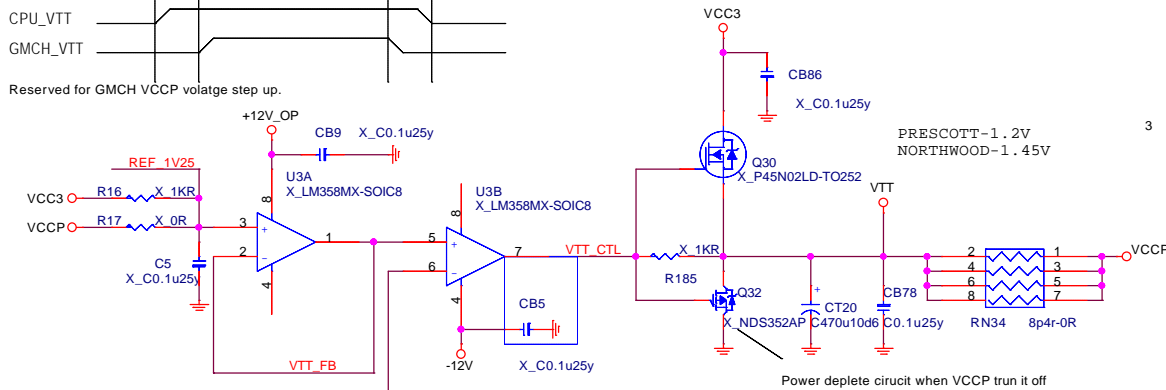


Intel reference GMCH VTT power circuit

Change R103 connected from Q55 source to drain to eliminate a floating connection when Q55 turn it off.

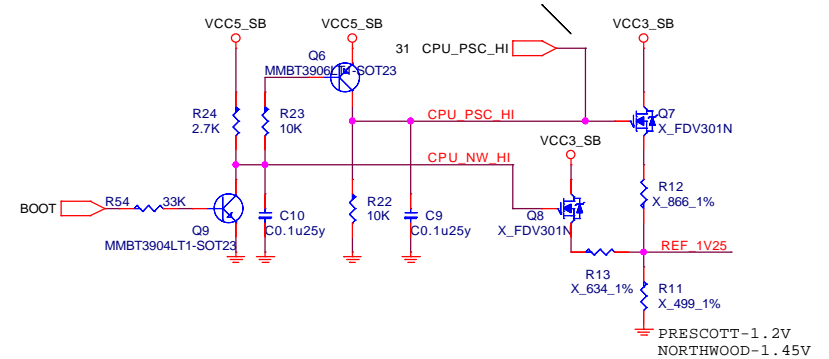


GMCH VTT Generator



Power deplete circuit when VCCP turn it off

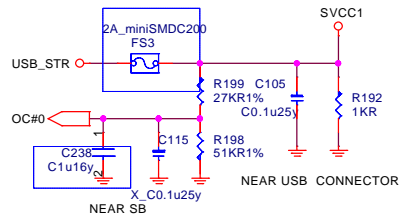
Bootstrap pin are input rather then output on Intel Prescott processor, either it's internal weak pull-up but still need to identify it can be sufficient driving capability for out side circuit. And the bootstrap pin power by core voltage so the outside circuit need to adjust the turn off voltage.



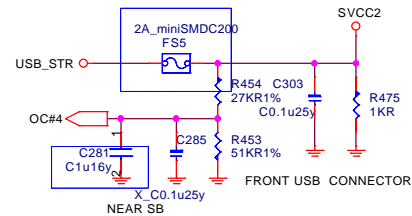
MICRO-STAR INT'L CO., LTD.

Title			
GMCH VTT Power Module			
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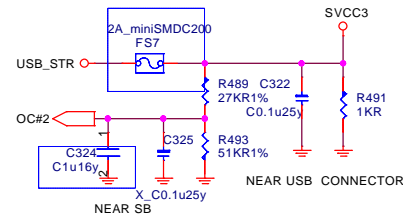
POWER CIRCUIT FOR USB PORT 0,1



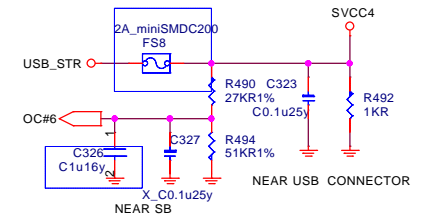
POWER CIRCUIT FOR USB PORT 4,5



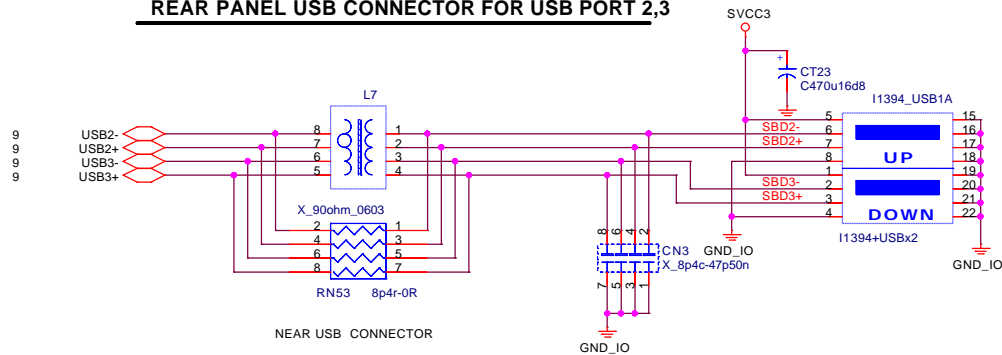
POWER CIRCUIT FOR USB PORT 2,3



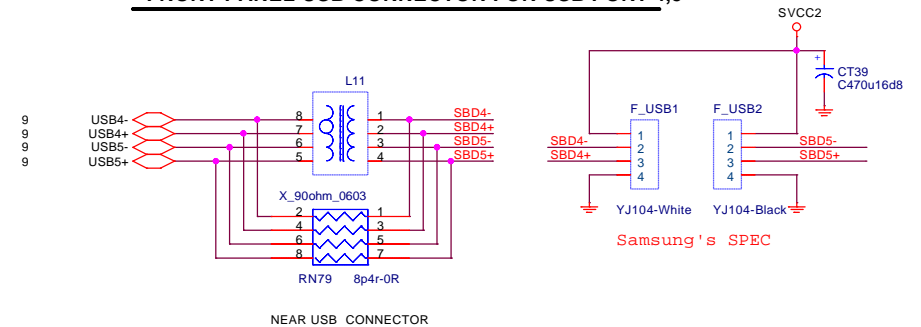
POWER CIRCUIT FOR USB PORT 6,7



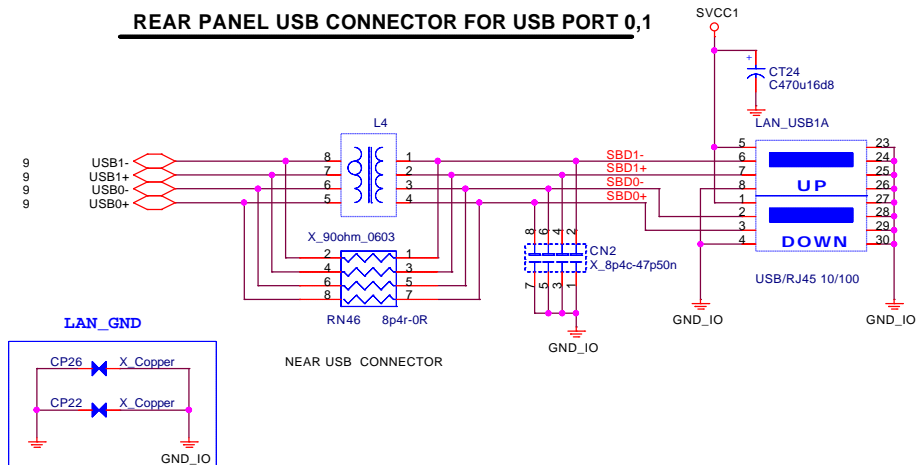
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



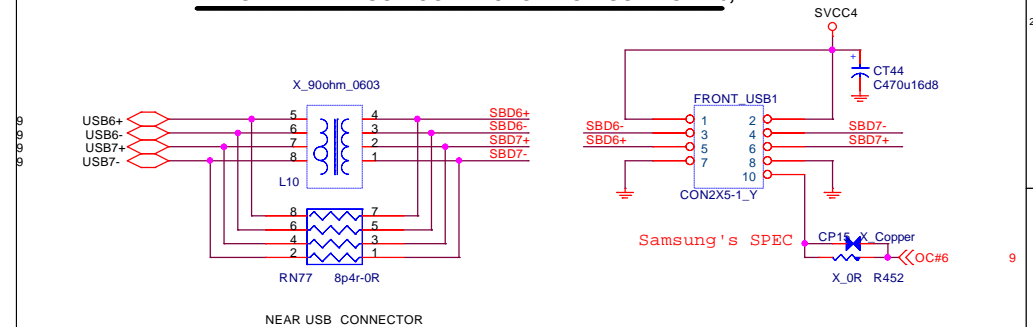
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

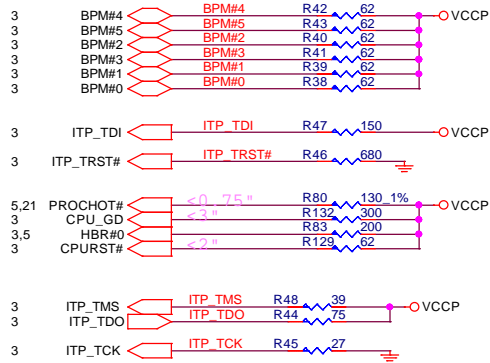


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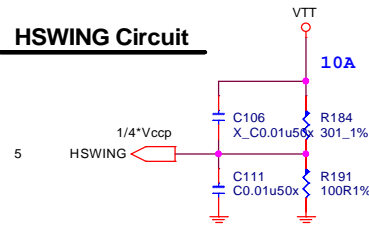
Title			
USB Connectors			
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CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



HSWING Circuit



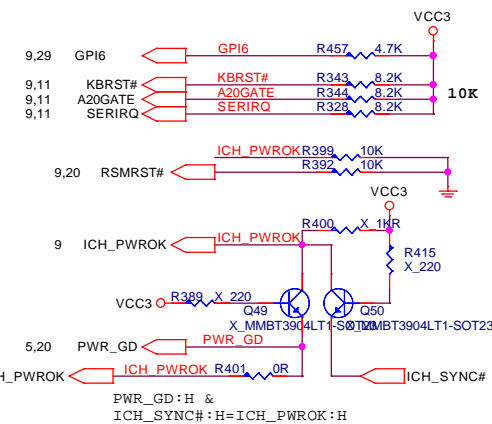
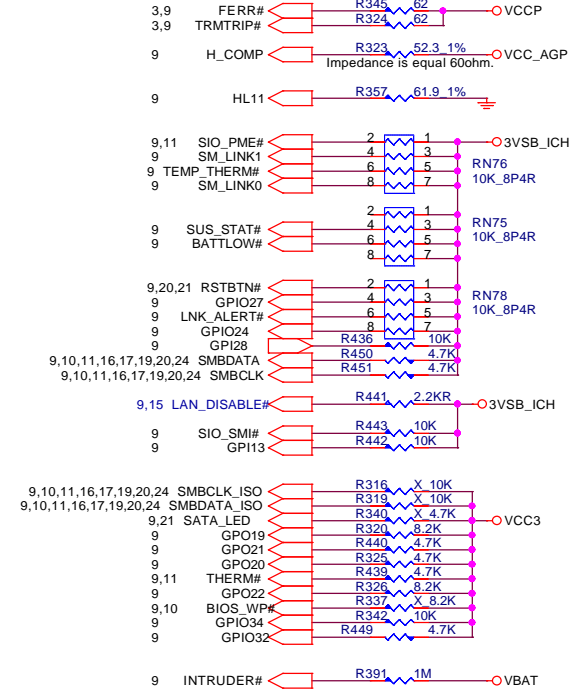
5VREF Sequencing Circuit



ICH5 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH5

Trace length is less than 3inches to ICH5.

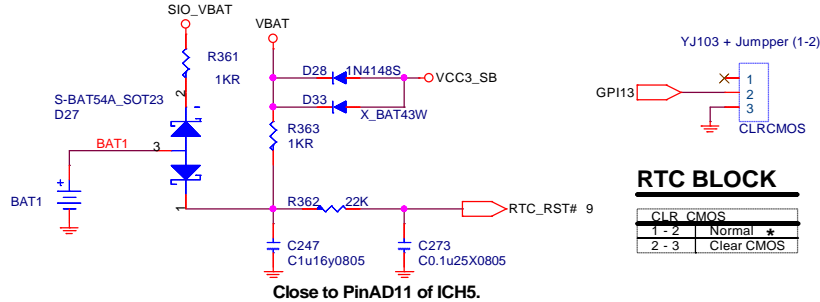
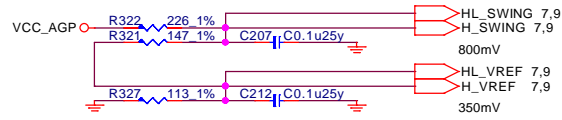
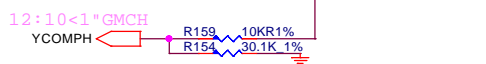
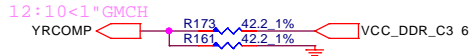
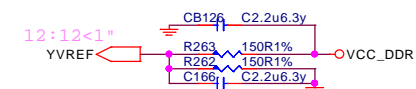
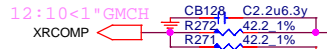


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Title
 CPU & GMCH & ICH5 PULL UP / DOWN RESISTORS

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 Abel/Totoro MS-7040

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RTC BLOCK

CLR_CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

Close to PinAD11 of ICH5.

ICH5

GPIO Pin	Type	Function
GPIO 0	I	ATADET0 (multifunction pin)
GPIO 1	I	ATADET1 (multifunction pin)
GPIO 2	I	PCI_IRQ#E (multifunction pin)
GPIO 3	I	PCI_IRQ#F (multifunction pin)
GPIO 4	I	PCI_IRQ#G (multifunction pin)
GPIO 5	I	PCI_IRQ#H (multifunction pin)
GPIO 6	I	Unused (multifunction pin)
GPIO 7	I	Unused (multifunction pin)
GPIO 8	I	SIO_PME# (multifunction pin)
GPIO 9	I	Unused (multifunction pin)
GPIO 10	I	Unused (multifunction pin)
GPIO 11	I	Unused (multifunction pin)
GPIO 12	I	SIO_SMI#
GPIO 13	I	Unused (multifunction pin)
GPIO 14	I	Unused (multifunction pin)
GPIO 15	I	Unused (multifunction pin)
GPIO 16	O	Unused (multifunction pin)
GPIO 17	O	Unused (multifunction pin)
GPIO 18	O	Unused (multifunction pin)
GPIO 19	O	Unused (multifunction pin)
GPIO 20	O	Unused (multifunction pin)
GPIO 21	O	Unused (multifunction pin)
GPIO 22	OD	Unused (multifunction pin)
GPIO 23	O	BIOS_WP# (multifunction pin)
GPIO 24	I/O	Unused (multifunction pin)
GPIO 25	I/O	LAN_DISABLE#
GPIO 27	I/O	Unused (multifunction pin)
GPIO 28	I/O	Unused (multifunction pin)
GPIO 32	I/O	Unused (multifunction pin)
GPIO 33	I/O	Unused (multifunction pin)
GPIO 34	I/O	Unused (multifunction pin)
GPIO 40	I	PREQ#4 (multifunction pin)
GPIO 41	I	Unused (multifunction pin)
GPIO 48	O	PGNT#4 (multifunction pin)
GPIO 49	OD	CPU_GD (multifunction pin)

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI slot 1-3, 1394
PCIRST#2	Super I/O, AGP slot
PCIRST_ICH5#	Northbridge, FWH
HDDRST#	Primary, Secondary IDE

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#G PIRQ#H PIRQ#E PIRQ#F	PCI_REQ#0 PCI_GNT#0	AD26	PCICLK0
PCI Slot 2	PIRQ#F PIRQ#G PIRQ#H PIRQ#E	PCI_REQ#4 PCI_GNT#4	AD25	PCICLK1
PCI Slot 3	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PCI_REQ#2 PCI_GNT#2	AD28	PCICLK2
1394	PIRQH	PCI_REQ#1 PCI_GNT#1	AD29	1394_PCLK

SIO

PIN NAME	USAGE	Input/Output	NOTES
GPIO10	UNUSED	INPUT	
GPIO11	UNUSED	INPUT	
GPIO12	UNUSED	INPUT	
GPIO13	UNUSED	INPUT	
GPIO14	UNUSED	OUTPUT	
GPIO15	VID5	INPUT	Low: VID add 0.0125V, High :by pass
GPIO16	UNUSED	OUTPUT	
GPIO17	UNUSED	OUTPUT	
GPIO20	UNUSED	OUTPUT	
GPIO21	SMBCLK_ISO	INPUT	SMBUS CLOCK
GPIO22	SMBDATA_ISO	INPUT / OUTPUT	SMBUS DATA
GPIO23	POWER_LED	OUTPUT	Default used MS-5
GPIO24	UNUSED	OUTPUT	
GPIO25	UNUSED	OUTPUT	IRRX
GPIO26	UNUSED	OUTPUT	
GPIO27	UNUSED	OUTPUT	
GPIO30	SLP_S3#	INPUT	S3 state indicator signal
GPIO31	PS_ON#	OUTPUT	Connector to Power Supply to turn on Power.
GPIO32	UNUSED	OUTPUT	
GPIO33	UNUSED	OUTPUT	
GPIO34	UNUSED	OUTPUT	
GPIO35	UNUSED	OUTPUT	

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A6H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

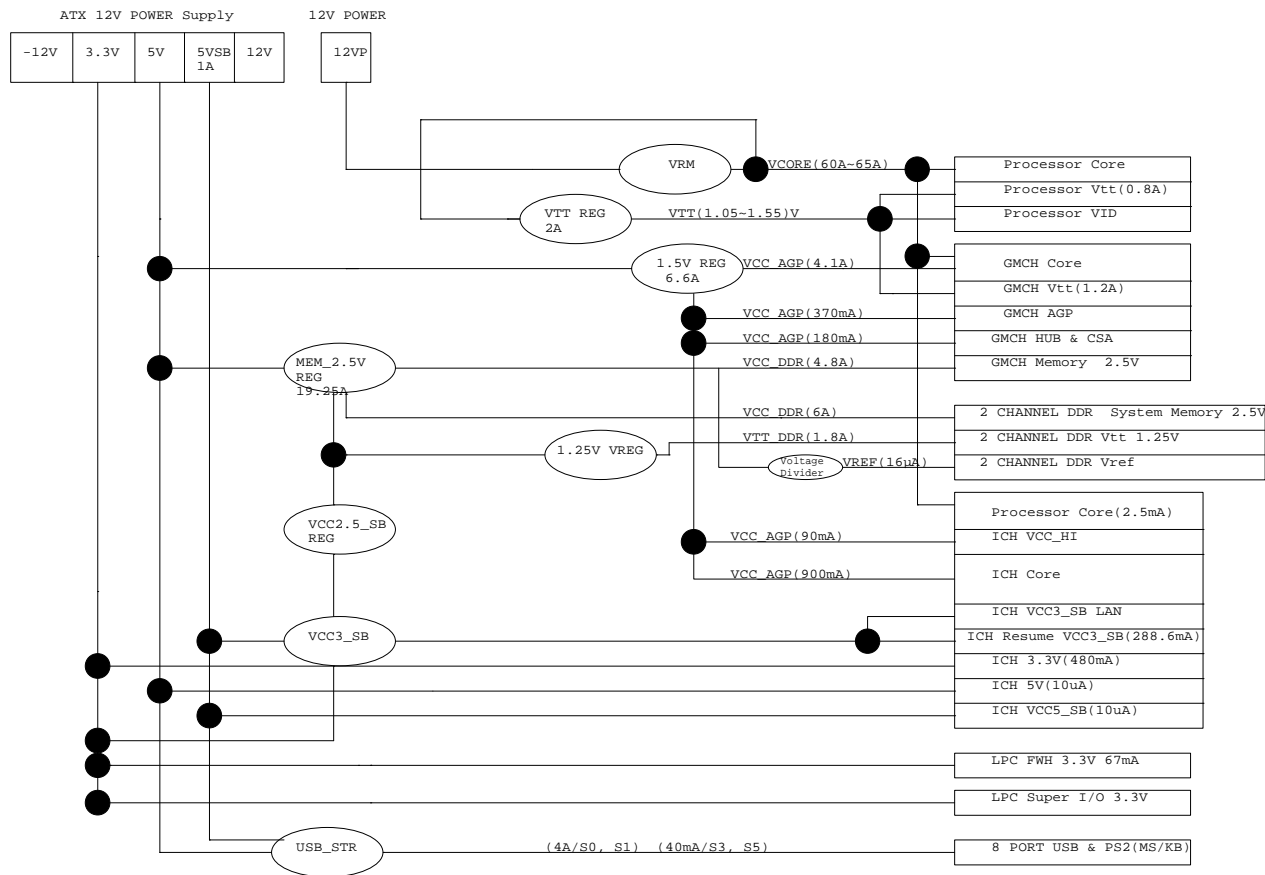
JUMPER SETTING

CLRCMOS	(1-2) NORMAL	(2-3) CLEAR
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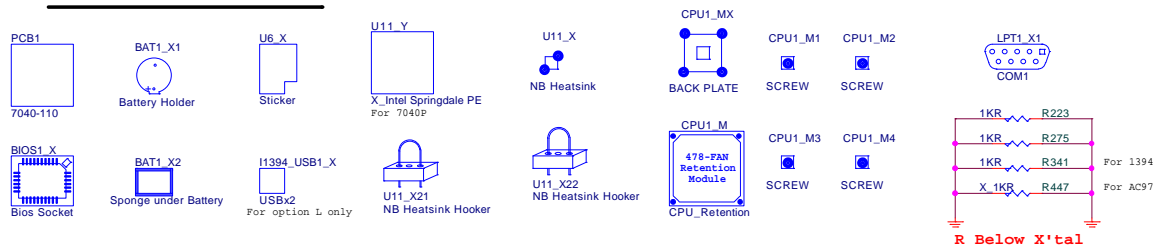
MICRO-STAR INT'L CO., LTD.

Title			
General Purpose Spec & JUMPER SETTING			
Size	Document Number	Rev	
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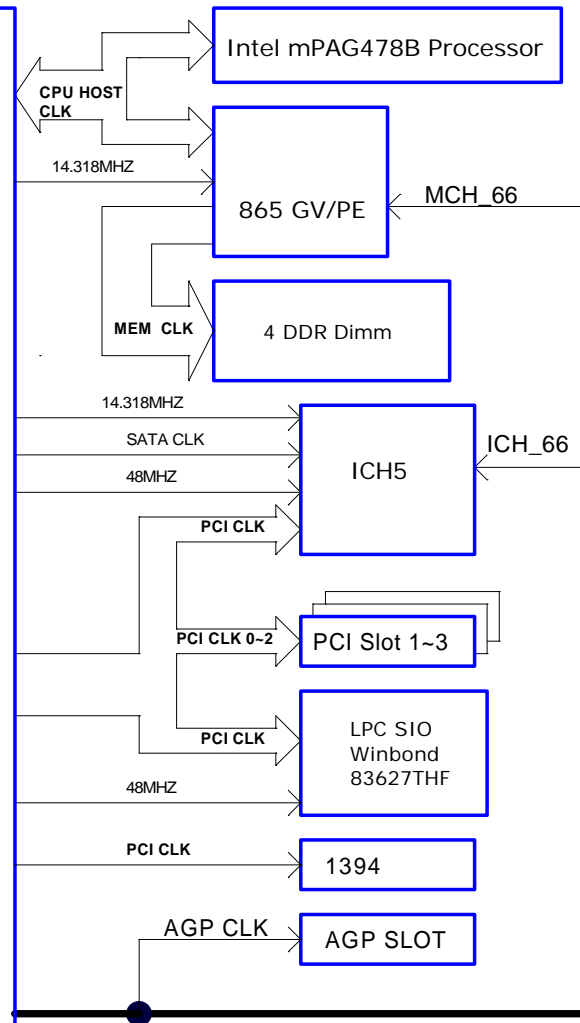
POWER DELIVERY MAP



7040-STD PART



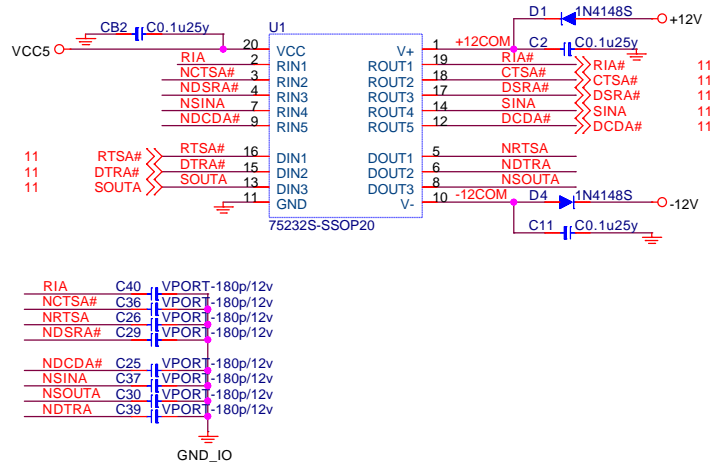
CLOCK GENERATOR



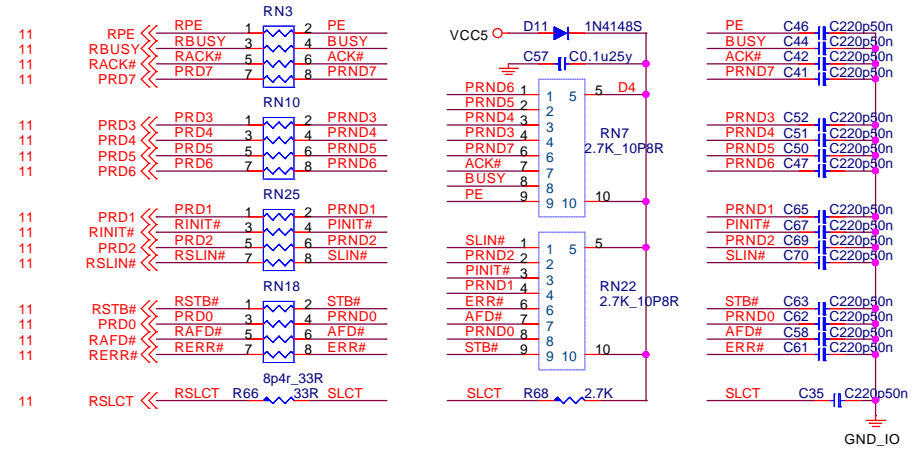
MICRO-STAR INT'L CO., LTD.

Title			POWER DELIVERY MAP & MANUAL PART
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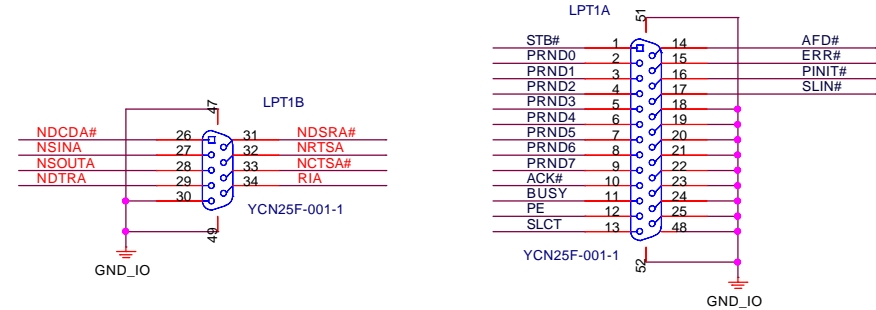
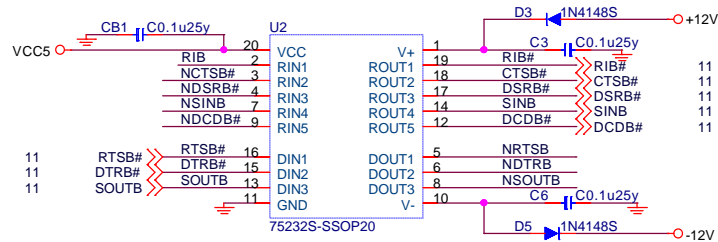
SERIAL PORT 1



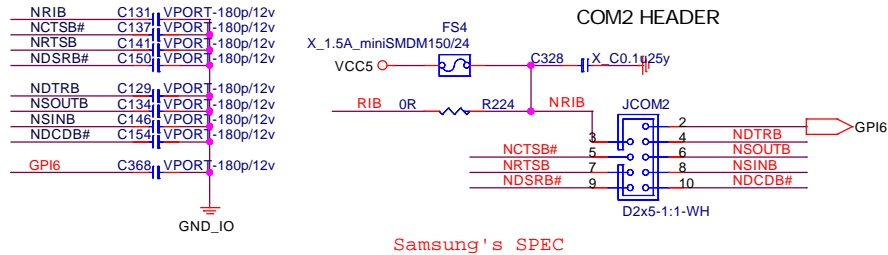
PARALLAL PORT



SERIAL PORT 2

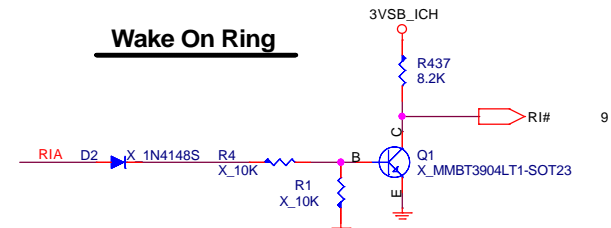


COM2 HEADER



Samsung's SPEC

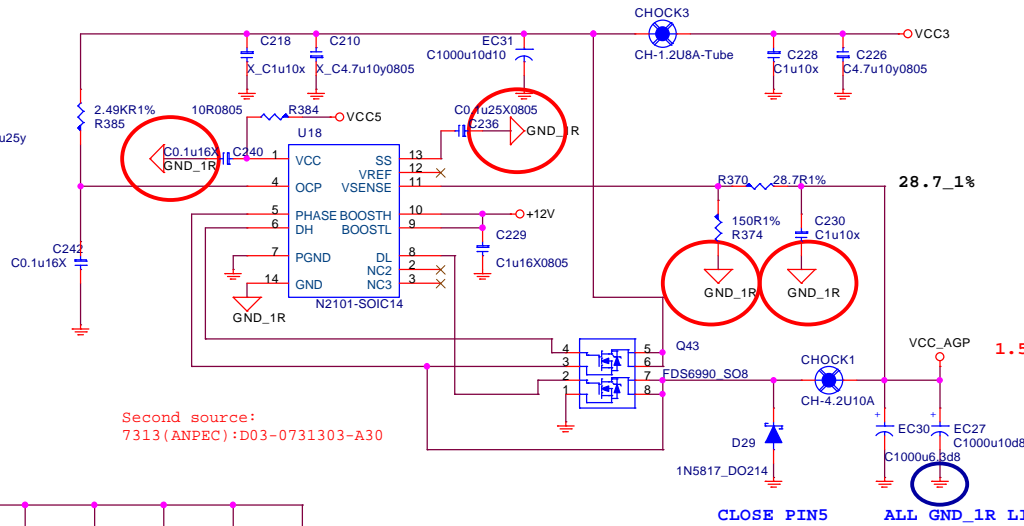
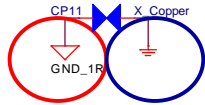
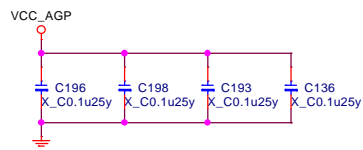
Wake On Ring



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Title			COM,LPT,RING WEAKER UP
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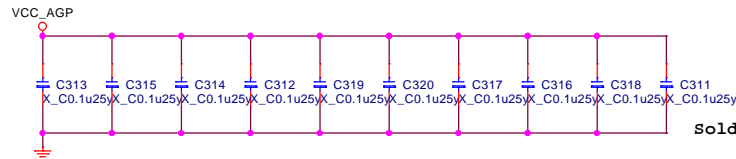
AGP Power

1.5V / 4A (NB) + 1A (SB) + 2A (AGP)

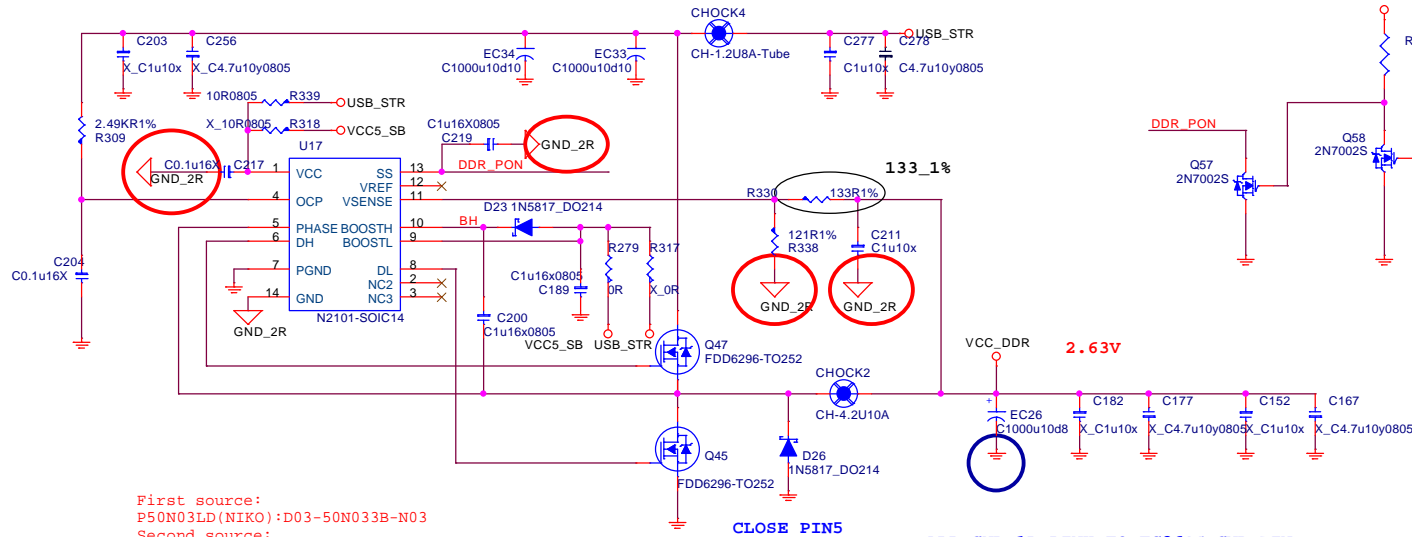
1.56V

CLOSE PIN5

ALL GND_1R LINK TO EC27'S GND PIN

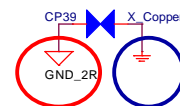
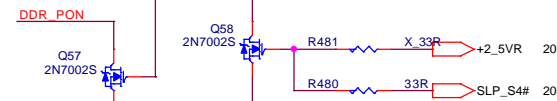


Solder side decoupling (5020)



DDR Power

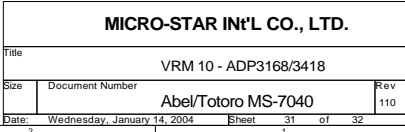
2.5V / 7A (DIMM) + 5.1A (NB)



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AGP & DDR POWER

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00A
1.D34 diode change to 1N5817 fixed gate driver voltage drop issue (Page 30).
2.Remove CNR for Samsung's SPEC (Page 22).
3.Add RN90 VTT connect to Vccp (Page 24).
4.Change JUSB1,2,3 for Samsung's SPEC (Page 25).
5.Add D36,D37 JCOM1 for Samsung's SPEC (Page 29).
6.Remove System Fan circuit for Samsung's SPEC (Page 18).
7.CT4,5,38,49,54 change to 1000u/10V for Samsung's SPEC (Page 25).
8.Add CT65 for Vcc5 ,CT66 for Vcc12 meet Samsung's SPEC (Page 25).
9.Add R933,934,935 clk gen NC resistor for Samsung's SPEC (Page 28).
10.Add power led for Samsung's SPEC (Page 21).
11.Remove IR & chasiss function for Samsung's SPEC (Page 21).
12.Change DDR switch power IC to USB_STR power and power on control by SLEEP_S4# (Page 30).

Oct. 31
1. Page 18 : Add system fan circuit.
2. Page 22 : add FS6 and connect P/S2 power to USB_STR.
3. Page 29 : make caps for COM2 separated, and add GP16 as detecting pin.
4. Page 25 : add SVCC3, SVCC4 power circuit for USB ports 2, 3, 6, 7.
5. Page 14 : Make R158, R246 stuffed.

Nov. 3
1. Page 22 : make C1 stuffed.
2. Page 29 : add C328 on net NRIB.
3. Page 25 : add CT44.
4. Page 9, 21, 26 : change COM2_DET# to SATA_LED.

100
Dec. 3
1. Page 13 : C265, C266 changed to 1uF 16V 0805: R466, R467 un-stuffed for 24MHz x'tal present.
2. Page 19 : CT33, CT37 changed to 10uF 25V EL SMD.
3. Page 18 : CB123, CB124, CB125, CB129, CB133, CB134, C183 un-stuffed for Springdale GV.
4. Page 8 : make net separated for pin F19, Y5, AA4, AB4, F7 and F8 and arrange corresponding caps.
5. Page 13 : lead MIC1_F to both rear and front connectors, and add R494.

Dec. 4
1. Page 31 : Use coppers for R71, R72, R73, R74 as substitute.
2. Stuff/add the following parts for EMI/ESD :
page 15 : C174, C205;
page 14 : C159, C100, C97, C93, C330, C331;
page 13 : C157, C158, C162 -- C165, C302, C310, C329;
page 11 : CB3, CB27;

Dec. 8
1. Reserve these for EMI/ESD : page 22 : C332, C333; page 12 C334 -- C348;
2. Page 25 : delete CP19, CP25, CP27 -- CP30, CP36, CP37 for EMI/ESD.
3. Chane the net from GND to GND_IO for EMI/ESD : page 23, 25 I1394 USB1; page 23 LAN_USB1;
page 22 : JKBSM1; page 29 : LPT1; and their corresponding accessary caps.
4. Page 13 : add C349, C351, v-port protection diodes.
5. Page 8 : make CB142, CB138, CB162, CB164 markable in location.
6. Page 10 : change R252, R253 to 33 ohm; reserve C350, R496; change C156 pin 1 to SIO48.
7. Page 12 : change R78, RN2 to 1K, but not stuffed.
8. Page 13 : change R438 to 47 ohm; make C282 stuffed 10pF; change C296, C299 to 100uF;
change R258, R259 to 33 ohm; add FB18, FB19; replace R474, R463 with FB20, FB21;
Codec CLK text; add R497, R498, FB22, FB23; R499, FB24, FB25, FB26;
add FB27 and change C300 to 100pF and net;
9. Page 14 : add R500.
10. Page 16 : change RN20 to 47 ohm.
11. Page 22 : stuff FB1; remove CP1.
12. Page 23 : connect U19 pin 74 to PCIRST#1.

Dec. 9
1. Page 15 : reserve C352, C353 for EMI.
2. Page 13 : AMP circuit added for Codec line-out.
3. Page 21 : add PROCHOT# CPU throttling circuit.
4. Page 18 : change SYS_FAN pin 1 to VCC, pin 2 to GND.

100
Dec. 10
1. Change the version to 10 directly.
2. Page 21 : change R506, R507 to 1% type.
3. Page 22 : add CP48 -- CP53 for EMI.
4. Page 10 : add C365; connect C350 to USB_48 by EMI.
5. Page 25 : make CP22, CP26 connected to GND and GND_IO by EMI.

Dec. 11
1. Page 30 : change R374 to 150 ohm 1%; change R277 to 191 ohm 1%.
2. Page 13 : add CP54; change C329 to GND.
3. Page 5 : change CT22 to 22u/10V 1206.
4. Move CB138, CB142, CB162, CB164 from page 8 to page 9.

Dec. 12
1. Page 13 : add R511, R512 and change MIC net; add EC39, EC40;
replace FB28, FB29 with R513, R514.
2. Page 31 : change R67 to 820 ohm; R65 to 33K ohm;R69 to 62K ohm; R84 -- R86 to 91K ohm;
C32 to 4.7u/35V 1206; C27 to 4700p; COILL -- 3 to 0.65u 30A.
3. Page 4 : change EC8, EC13, EC16 to 330u/2v SP.

Dec. 15
1. Page 19 : add C366.
2. Page 13 : change R501, R503 to 39K; change R502, R504 to 47K; change R511 net.
3. Page 29 : not stuff FS4, C328.
4. Page 23 : change EC32 to 0805 size.
5. Page 15 : change RN65, R288, R292 to 0402 size.
6. Page 13 : change C291 to 0.01u; page 10 : stuff R444.
7. Page 31 : delete CP40 -- CP43 : stuff R71, R72.

Dec. 16
1. Page 10 : delete redundant LP3 -- LP10; change CT27 to 10u/10V 1206.
2. Page 14 : change RN70, R398 to 0402 type.
3. Page 12 : stuff C334 -- C348; add C367 by EMI.
4. Page 29 : add C368 by EMI; change COM2 V-port cap to GND_IO.
5. Page 12 : delete R140, R144; change R147, R149 to 0402.
6. Page 31 : delete R57, R30, R37, R25, Q15, Q11, and connected VID_GD to U7 pin 11.
7. Page 13 : add R515 -- R519 by EMI.

Dec. 17
1. Page 11 : exchange nets for PWM_CPU, CPU_FAN1 and PWM_SYS, SYS_FAN1.
2. Page 18 : change CT6, CT43 to 10u 25V.
3. Page 8 : not stuff R426.
4. Page 13 : change R434 to 33 ohm.
5. Page 12 : change C334 -- C348 to 100p.

110
Dec. 31
1. Page 13 : replace R438, R434 with FB28, FB29; change C271, C282 to 22p; add FB30;
add R520; all by EMI.
2. Page 14 : change C93, C97 to 1000p 16V 0402; delete R500; add C371, C372 by EMI
3. Page 10 : connect MH7 pin 2, 3, 4 to GND; add C369, C370; change CN4 to 40p;
stuff C120, C116, C119, C151, C350, C365 10p; stuff C156 22p; stuff CN4;
replace R250 with FB31; replace RN63 with R521, R522, T523;
add C373 -- C377; all by EMI
4. Page 26 : reserve D33.
5. Page 12 : change D15, D16 to BAV99 and their nets by EMI.
6. Page 26 : change C105, C303, C322, C323 to 0.1u.

Jan. 5
1. Page 10 : add C378.

Jan. 9
1. Page 28 : not stuff R447, the R under AC97 x'tal.
2. Page 20 : change R307, R308 to 470 ohm.

Jan. 12
1. Page 21 : delete Q27, Q28, Q60, R162, R163, R105; add D34, D35, D36;
change R380 to 0805 and net to VCC5; reserve R524.
2. Page 20 : change R307, R308 to 330 0805.
3. Page 30 : change R385 to 2.2K ohm.
4. Page 13 : change C197 to 1u and net to VREF_OUT.
5. Page 12 : change FB9, FB10, FB11 to 0.1uH 300mA.

Jan. 13
1. Page 30 : change R385, R309 to 2.2K 1% 0603.
2. Page 13 : reserve R525.
3. Page 10 : replace CN4 with C379, C380, C381.

Jan. 14
1. Page 30 : change R385, R309 to 2.49K 1%.
2. Page 28 : change PCB1rev.110.

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